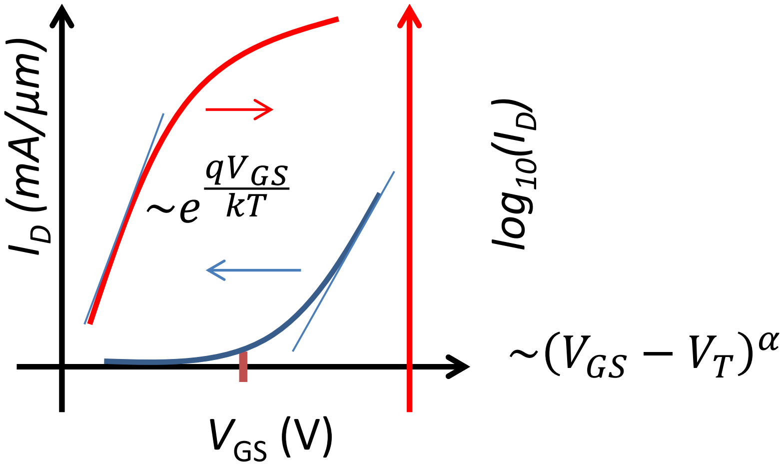
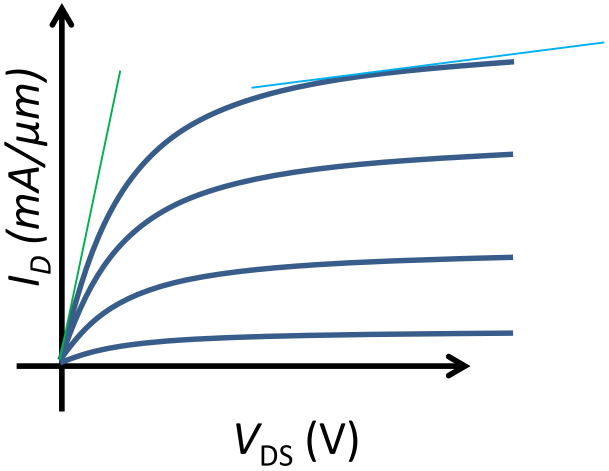
Lecture 2 –Devices and Circuits

- Basic Devices (39-82)
- Fundamental Device metrics
- MOS 1D Electrostatics
- Quantum/semiconductor capacitance
- CMOS Scaling Basics

Key Transistor Metrics:



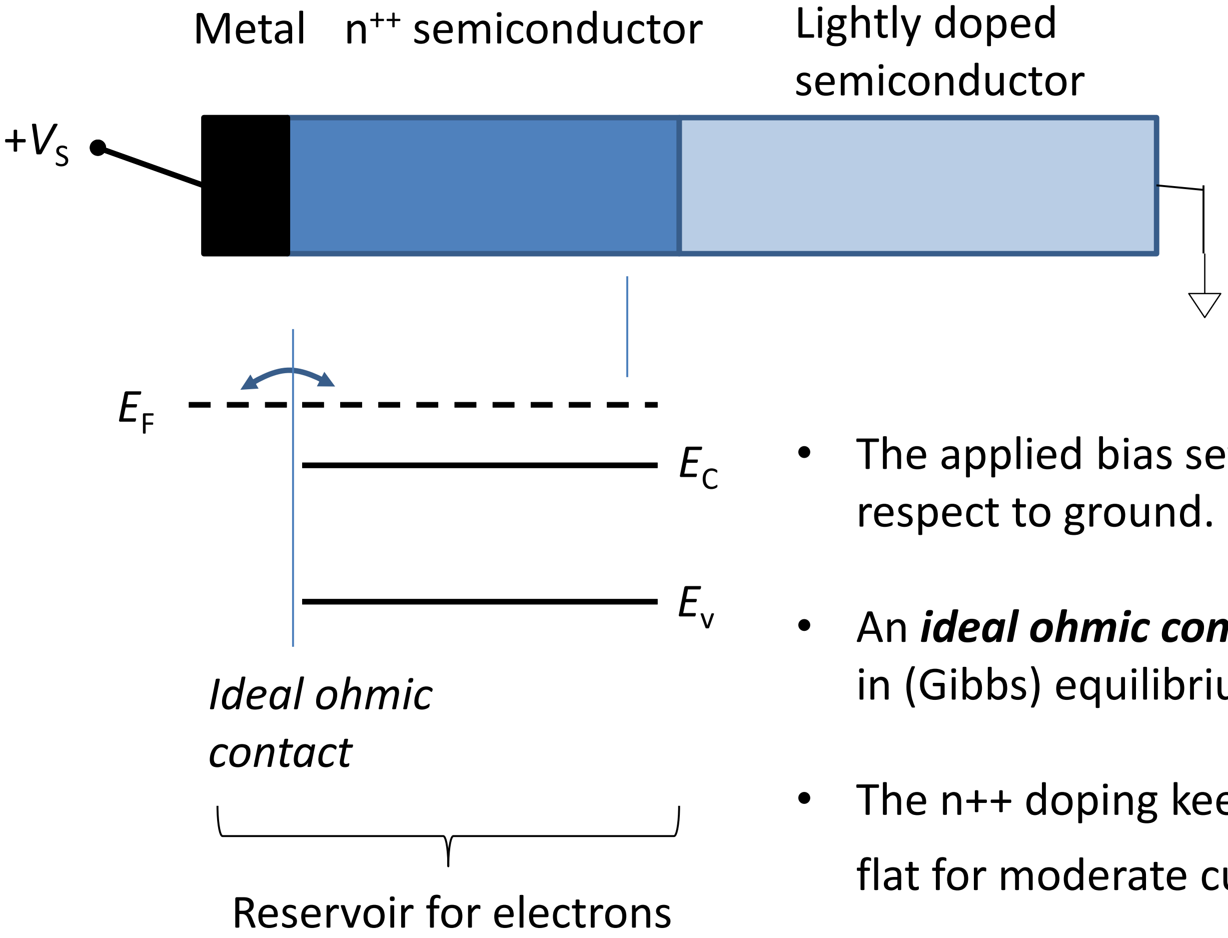


- Inverse subthreshold slope: (mV/decade)
- Drain Induced Barrier Lowering: mV/V
- Threshold Voltage
- On resistance R_{on}
- Transconductance (g_m) and on-current
- Output conductance: g_d

I_{off} (V_{gs}=0 – set by V_T)
HP=100 nA/μm
GP=1 nA/μm
LP=100 pA/μm
ULP=

I_{on}
0.1-1 mA/μm at
V_{DD}=V_{GS}=0.5-1V

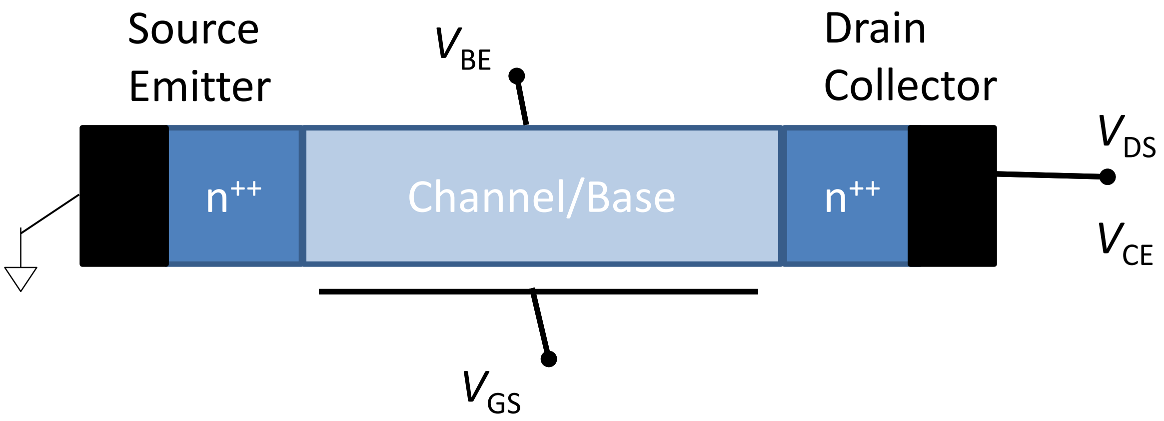
Reservoir



- The applied bias sets the metal fermi level with respect to ground. (Electric potential <->)
- An ***ideal ohmic contact*** keeps the semiconductor in (Gibbs) equilibrium with the metal <-> Equal E_F
- The n++ doping keeps the semiconductor bands flat for moderate current densities ($\frac{dE_f}{dx} = \frac{J}{\mu_n n}$)

Applied voltage – this shifts (E_F and E_C) by V

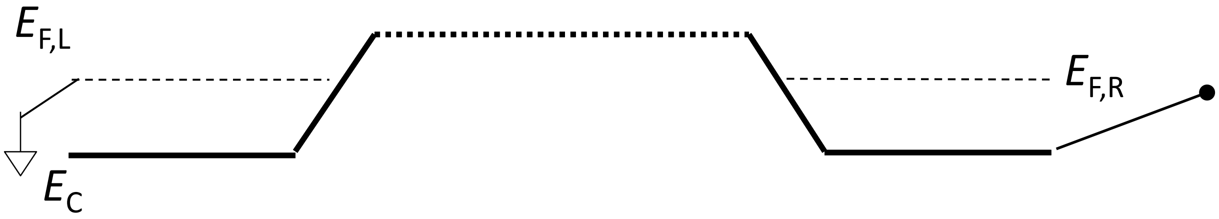
General Transistor Model



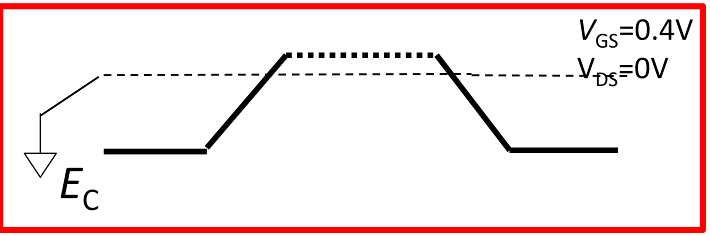
Ideal transistor the potential energy of the channel is *only* controlled by the gate/base terminal.

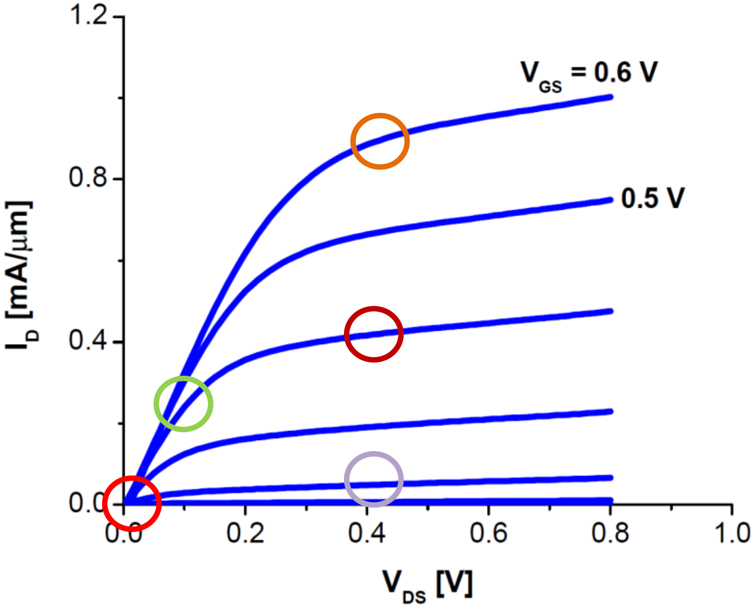
HBT – direct control of $E_{C,\text{channel}}$

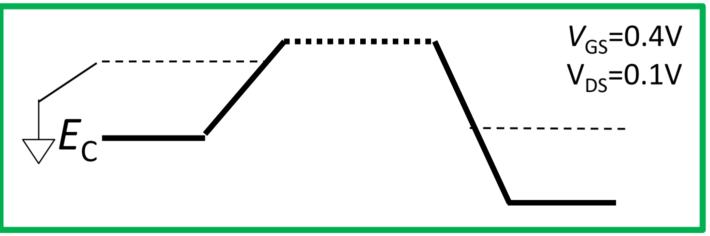
FET – indirect control of $E_{C,\text{channel}}$

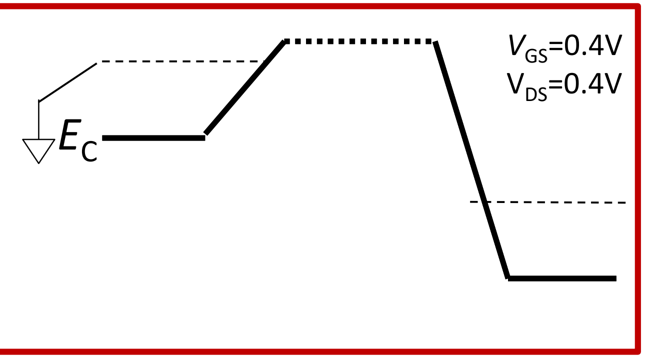


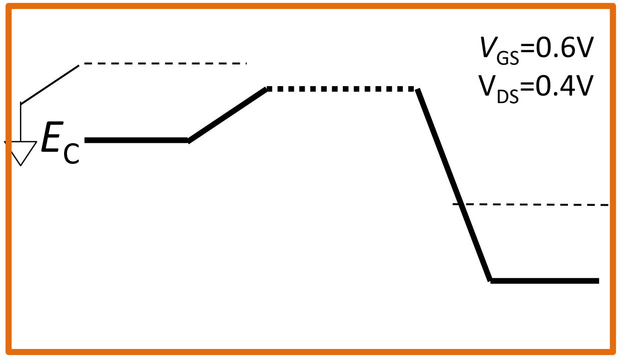
General Thermionic Transistor Model

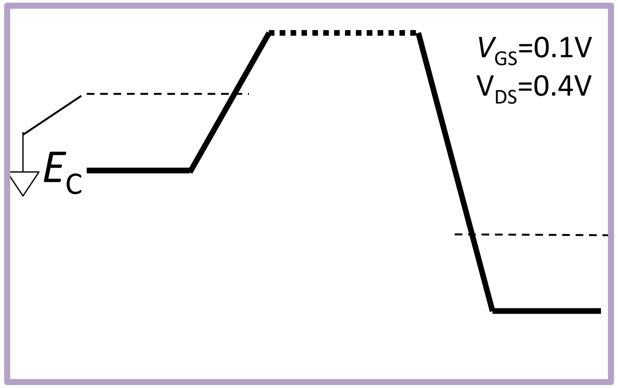




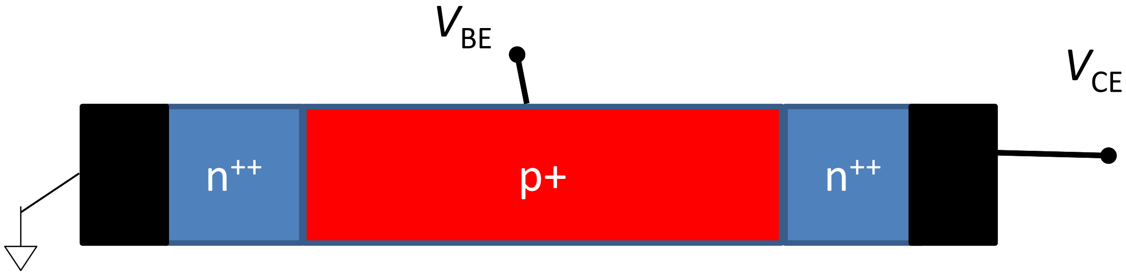








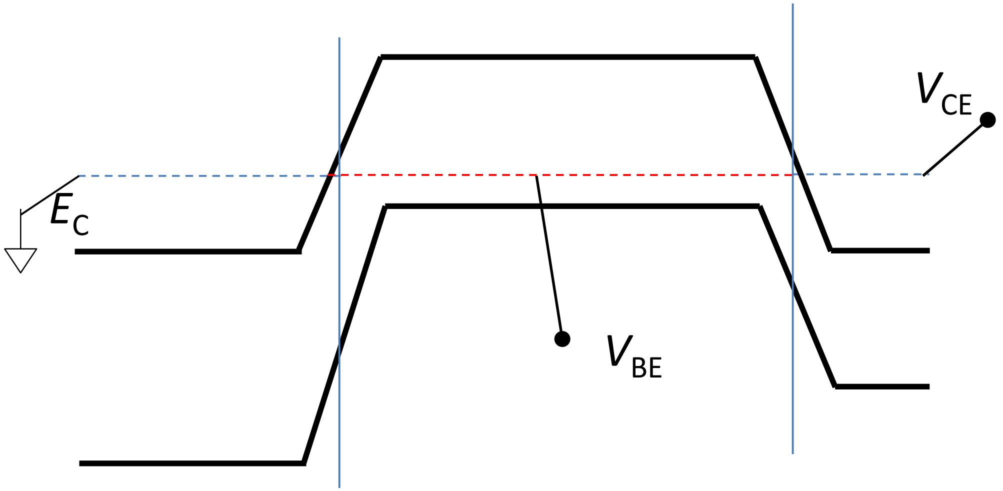
Bipolar Transistor Realization

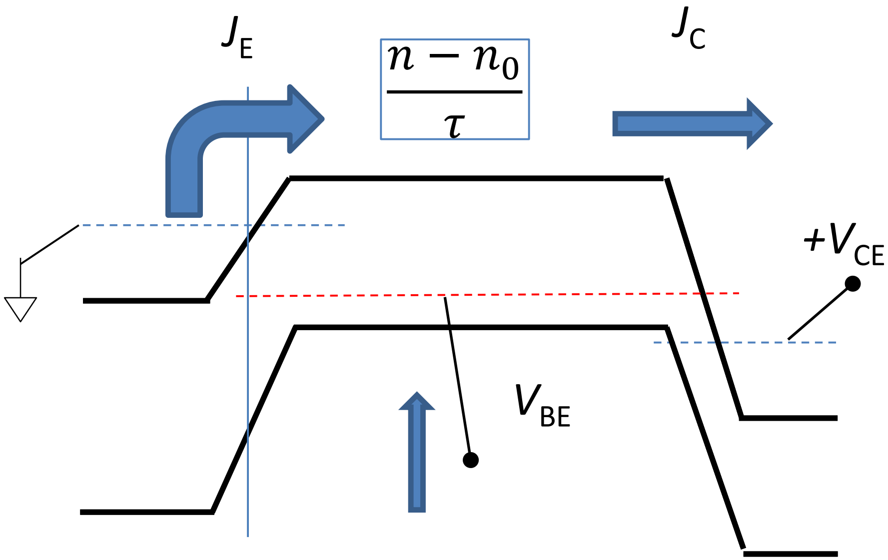


The base is a p+ region
The base terminal is connected directly to the base

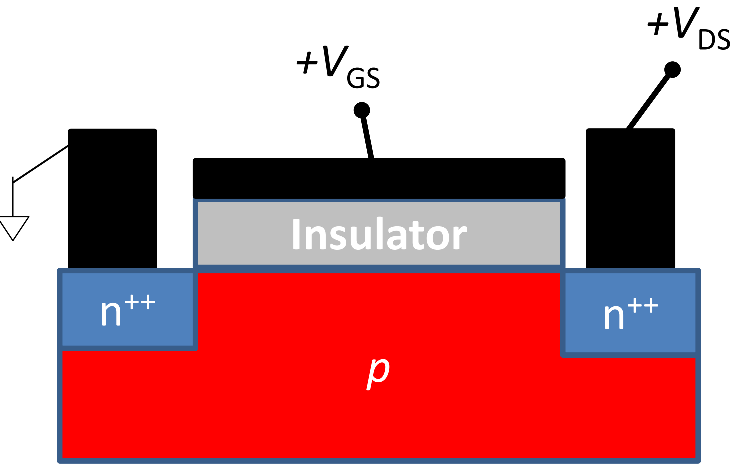
This constitutes a reservoir for ***holes*** – not for electrons

- No ε-field
- Diffusion with recombination
- Recombination: **base current**

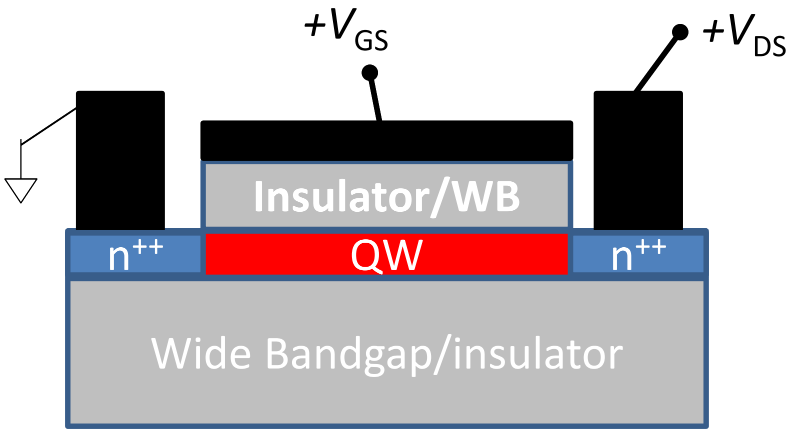




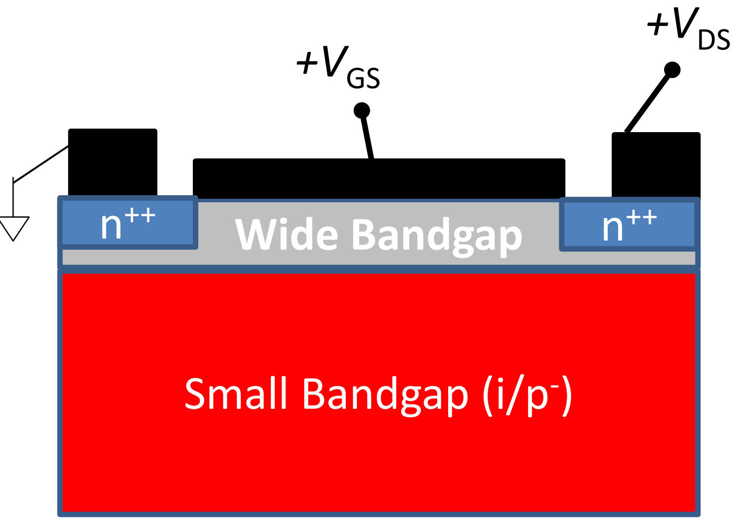
Field Effect Transistors - realization



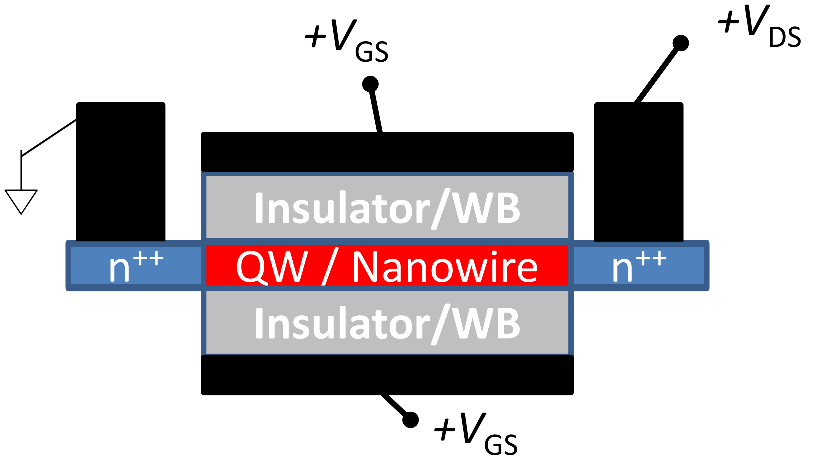
Traditional Si-MOSFET



Quantum Well HEMT /SOI MOSFET/
Graphene FET…

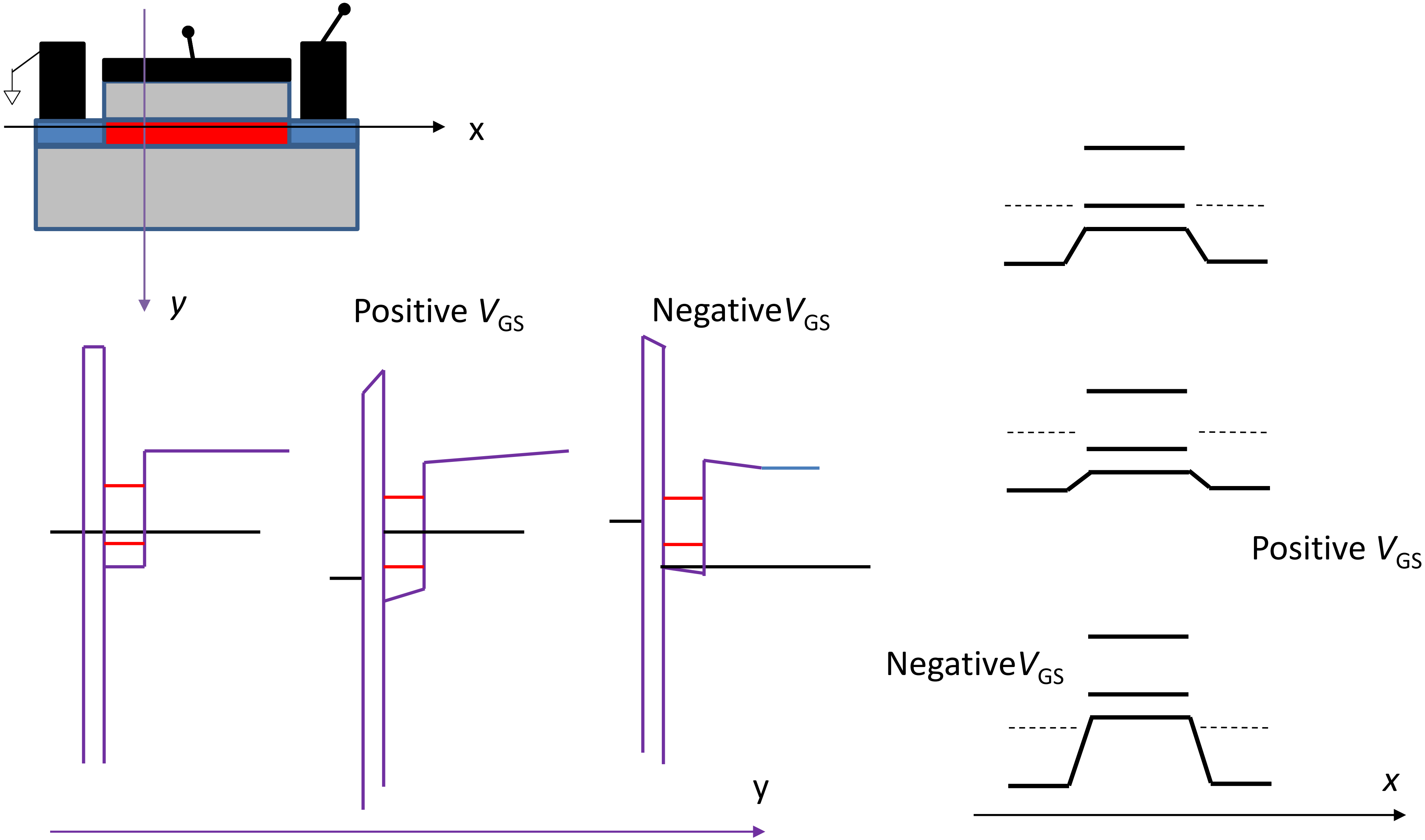


Traditional HEMT

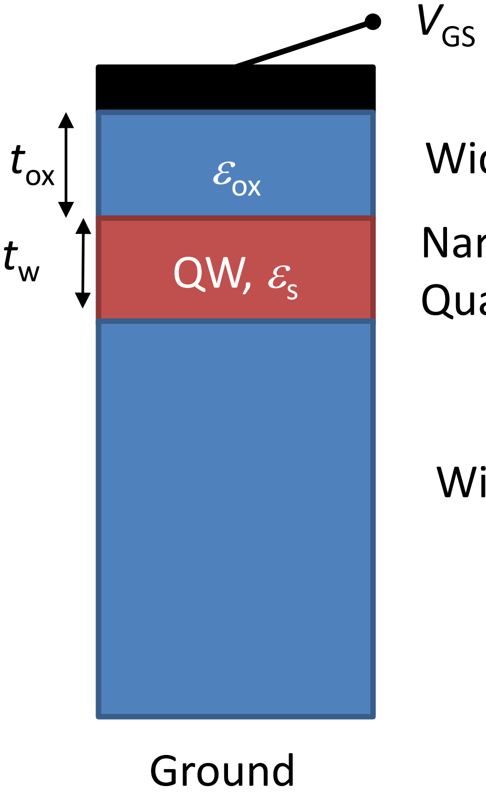


FinFET / Nanowire FET / Carbon Nanotube FET

Field Effect Transistors – indirect channel potential control



2D Field Effect Transistors



Wide Band Gap / Insulator

Narrow Band Gap,
Quantum Well

Wide Band Gap / Insulator

Typical Thickness:
t_{ox} 2-10 nm

Thick enough to prevent tunneling from QW to the gate.
Thin to prevent short channel effects.

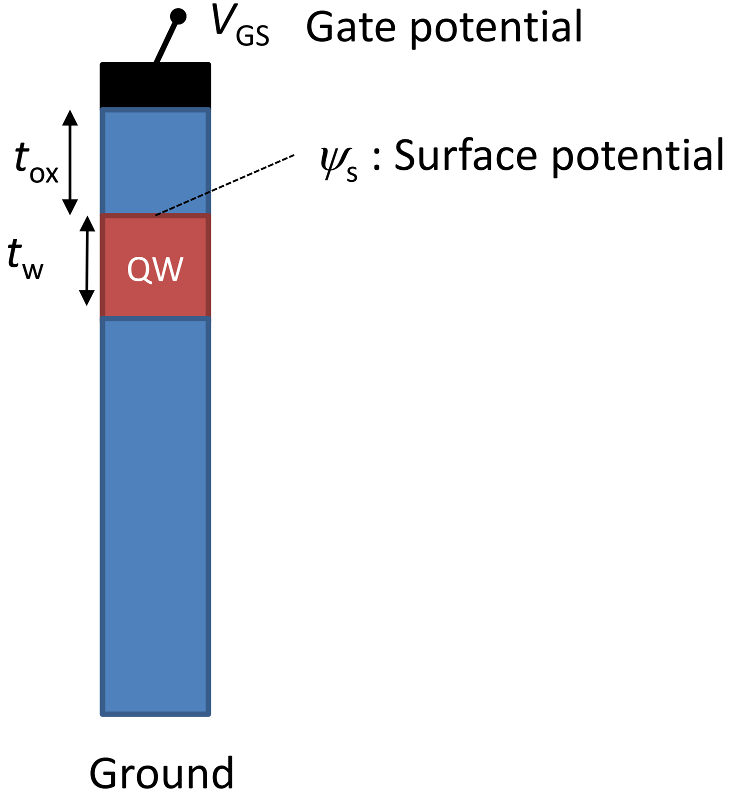
Typical Thickness:
t_w 0.5-10 nm

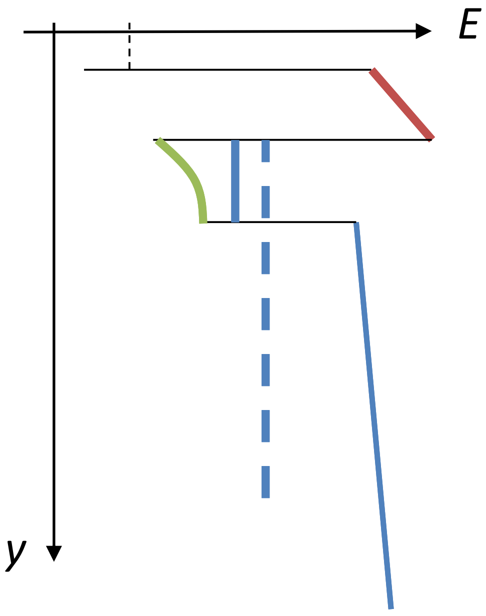
Thick enough to keep surface roughness under control. ($\mu_n \sim 1/L_W^6$)
Thin to prevent short channel effects.

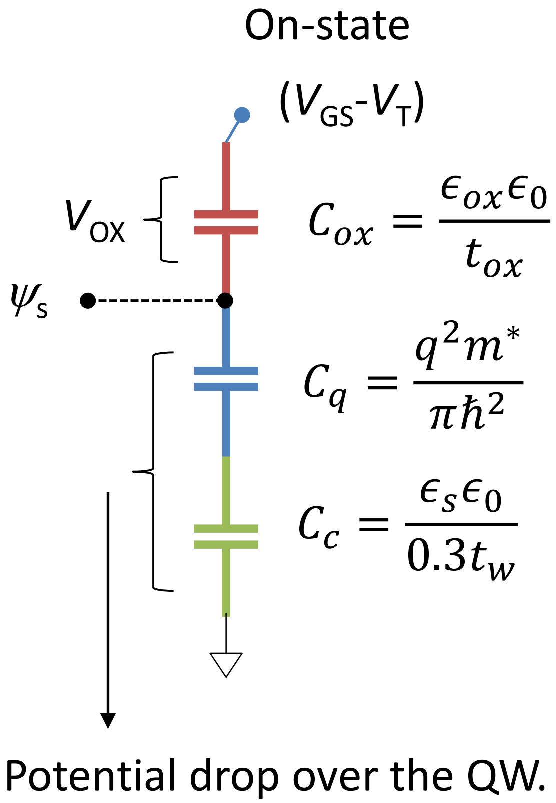
We will demonstrate that the QW charge can be written as:

$$qn_s = C_G(V_{GS} - V_T)$$

2D Field Effect Transistors







$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}}$$

$$C_q = \frac{q^2 m^*}{\pi \hbar^2}$$

$$C_c = \frac{\epsilon_s \epsilon_0}{0.3 t_w}$$

V_{GS} below V_T : Off $\quad qn_s \approx N_{2D} e^{\frac{q}{kT}(V_{GS}-V_T)} \approx 0$

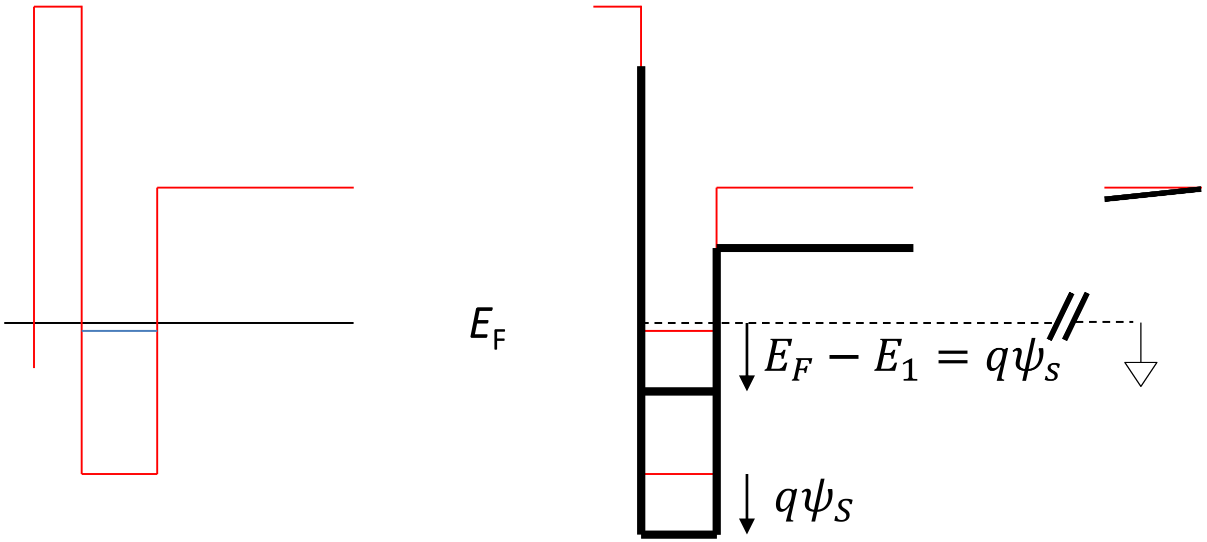
V_{GS} above V_T : On $\quad qn_s = C_G(V_{GS}-V_T)$

$$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_q} + \frac{1}{C_c}$$

Quantum / Semiconductor Capacitance

$$C_q = \frac{q^2 m^*}{\pi \hbar^2}$$

$$Q = CV$$



$$E_F - E_1 = q\psi_s$$

$$q\psi_s$$

$$\frac{d^2}{dx^2}V(x) = \frac{qn_s}{\epsilon_s \epsilon_0} \approx 0$$

If the induced charge in the quantum well is small: E_C remains ~ flat around the well

On-state: E_F-E_1>>0

Quantum Well Charge: $n_s = N_{2D} F_0(\eta_F) \approx \frac{m^*}{\pi \hbar^2}(E_F - E_1)$

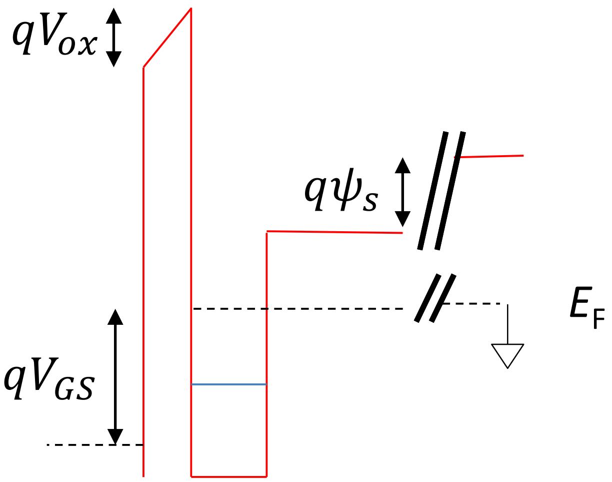
$$qn_s \approx \frac{q^2 m^*}{\pi \hbar^2}\psi_s = C_q \psi_s$$

V_T=0V

Quantum / Semiconductor capacitance:
q(E_F-E_1) needs to increase by $\frac{qn_s}{C_q} = \psi_s$.

$$C_s = q^2 \int_0^\infty D\left(-\frac{\partial f}{\partial E}\right) dE = q^2 \langle D(E_F) \rangle$$

Oxide Capacitance



+ V_{ox} -

$Q = qn_s$

$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}}$$

$$Q = CV$$

Potential drop over the oxide: $V_{ox} = \dfrac{qn_s}{C_{ox}}$

Total Potential drop: $V_{GS} = V_{ox} + \psi_s = \dfrac{qn_s}{C_{ox}} + \dfrac{qn_s}{C_q} = \dfrac{qn_s}{C_G}$

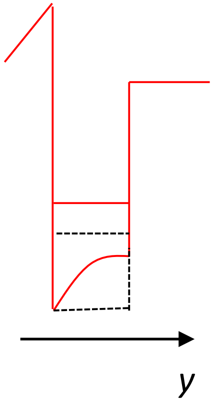
$$\boxed{qn_s = C_G V_{GS}}$$

Total Gate Capacitance: $\dfrac{1}{C_G} = \dfrac{1}{C_{ox}} + \dfrac{1}{C_q}$

V_T=0V

Charge Centriod Capacitance

There is charge qn_s inside the quantum well



$$\rho(y) \approx \frac{-qn_s}{t_w}$$

$$\varepsilon(t_W) = 0$$ All charge inside the QW

$$\varepsilon(x) = \frac{qn_s}{\epsilon_s\epsilon_0}(1 - \frac{y}{t_w})$$

$$\Delta V(x) = \frac{qn_s}{\epsilon_s\epsilon_0}(\frac{y^2}{2t_w} - y)$$

$$C_c = \frac{\epsilon_{ox}\epsilon_0}{0.28t_w}$$

$$Q = CV$$

Also gives C_{ox}

$$\varepsilon(0^+) = \frac{qn_s}{\epsilon_s\epsilon_0}$$

$$D(0^+) = D(0^-)$$

$$\varepsilon(0^-) = \frac{qn_s}{\epsilon_{ox}\epsilon_0}$$

$$V_{ox} = \varepsilon(0^-)t_{ox}$$

$$= qn_s\frac{t_{ox}}{\epsilon_{ox}\epsilon_0}$$

This leads to a *upward shift* of E_1

From first order perturbation theory:

$$\Delta E \approx \langle\Psi_1|qV(x)|\Psi_1\rangle = \frac{q^2n_s}{\epsilon_s\epsilon_0}\frac{2}{t_w}\int_0^{t_w}\sin^2\left(\frac{y\pi}{t_w}\right)\left(\frac{y^2}{2t_w} - y\right)dy = \cdots =$$

$$\Delta E = \underset{\overset{\uparrow}{(?)}}{2}q^2n_s\frac{t_w}{\epsilon_s\epsilon_0}\underbrace{\frac{1}{12}\left(2 - \frac{3}{\pi^2}\right)}_{\approx 0.14}$$

To obtain the same n_s: we need to add an extra $\Delta\psi_s$!

$$\Delta\psi_s = qn_s\frac{1}{C_c}$$

V_T=0V

n_s : Above / Below V_T

$$V_{GS} = V_{ox} + \psi_s' + \Delta\psi_s$$

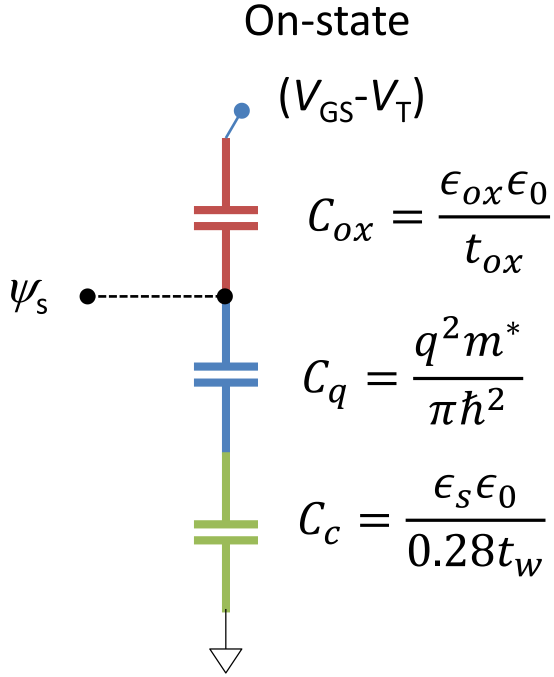
$$V_{GS} = \frac{qn_S}{C_{ox}} + \frac{qn_S}{C_q} + \frac{qn_S}{C_c} \qquad \frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_q} + \frac{1}{C_c}$$

Sub threshold: $E_F < E_1$. n_s becomes small.

$$V_{ox} \approx 0V \quad \Delta\psi_S \approx 0V \quad \longrightarrow \quad \psi_S \approx V_{GS}$$

$$n_s = N_{2D}F_0(\eta_F) \approx N_{2D}e^{\frac{E_F - E_1}{kT}} = N_{2D}e^{\frac{V_{GS}}{kT}}$$

Below V_T – exponentially decreasing n_s



$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}}$$

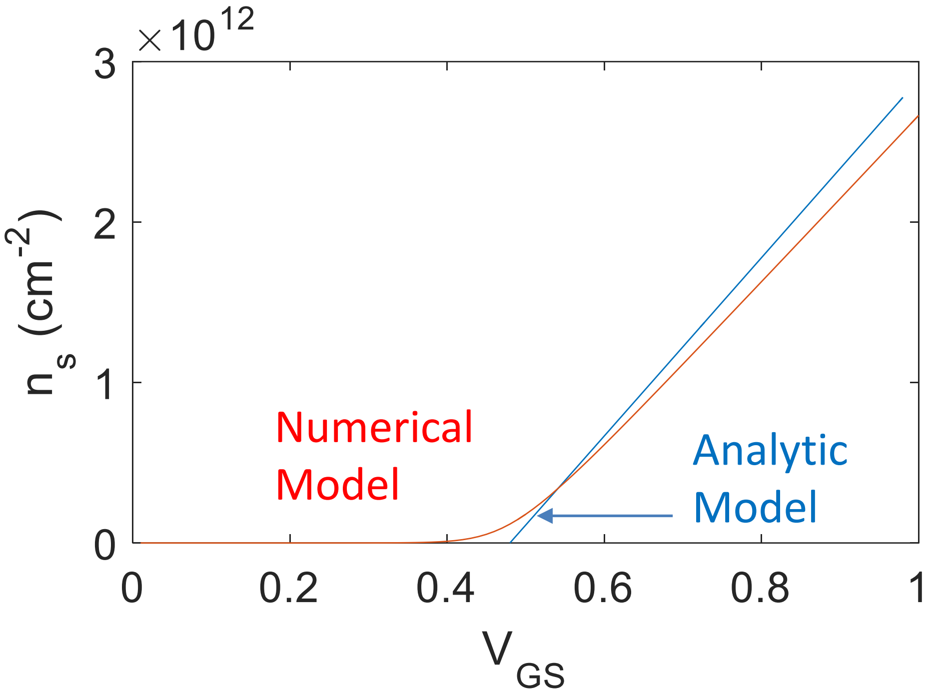
$$C_q = \frac{q^2 m^*}{\pi\hbar^2}$$

$$C_c = \frac{\epsilon_s\epsilon_0}{0.28t_w}$$

The effect of C_q and C_C can be modeled as an effective thicker t_{ox}. $C_G = \frac{\epsilon_{ox}\epsilon_0}{t_{ox} + \Delta t_{ox}}$

V_T=0V

2D MOSFET : Analytic / 1D Schrödinger/Possion Comparison



$$n_s = C_G(V_{GS} - V_T)$$

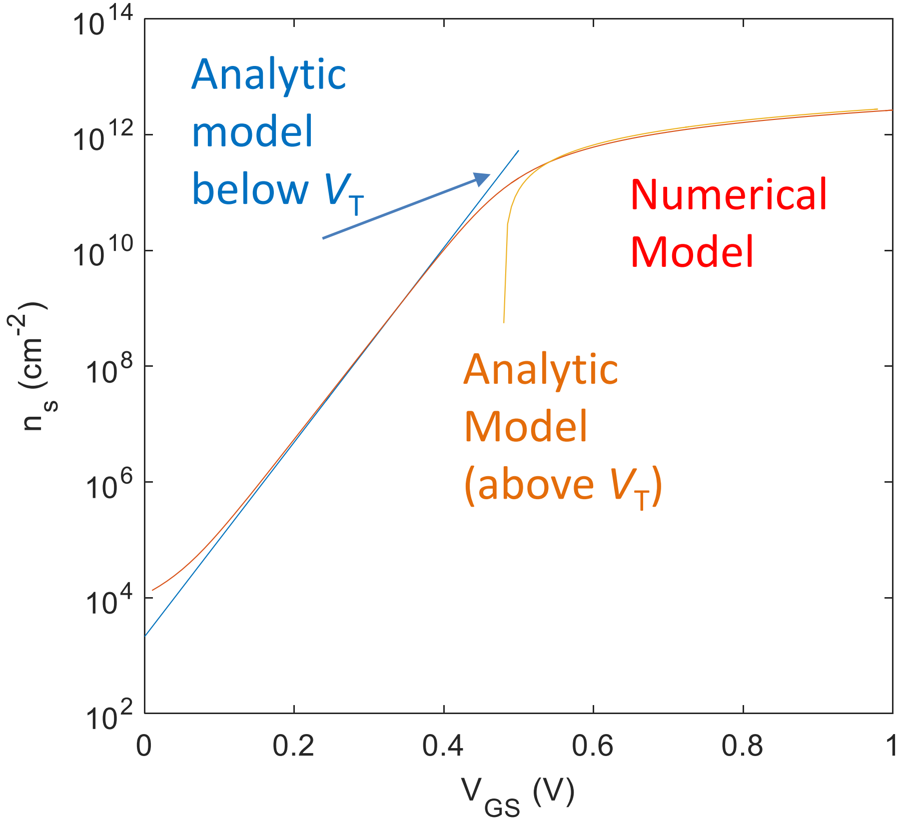
$$\phi_b = 5eV$$
$$\Delta E_C = 4.7eV$$
$$E_1 = 0.16\ eV$$

$$V_T = 0.46\ V$$

t_{ox}=5 nm
t_w=10 nm
$m^*=0.023m_0$

+The model accurately predicts $n_s(V_{GS})$ above V_T!
-Not accurate below V_T
-Only using the EMA

2D MOSFET : Analytic / 1D Schrödinger/Possion Comparison



t_{ox}=5 nm

t_w=10 nm

$m^*=0.023m_0$

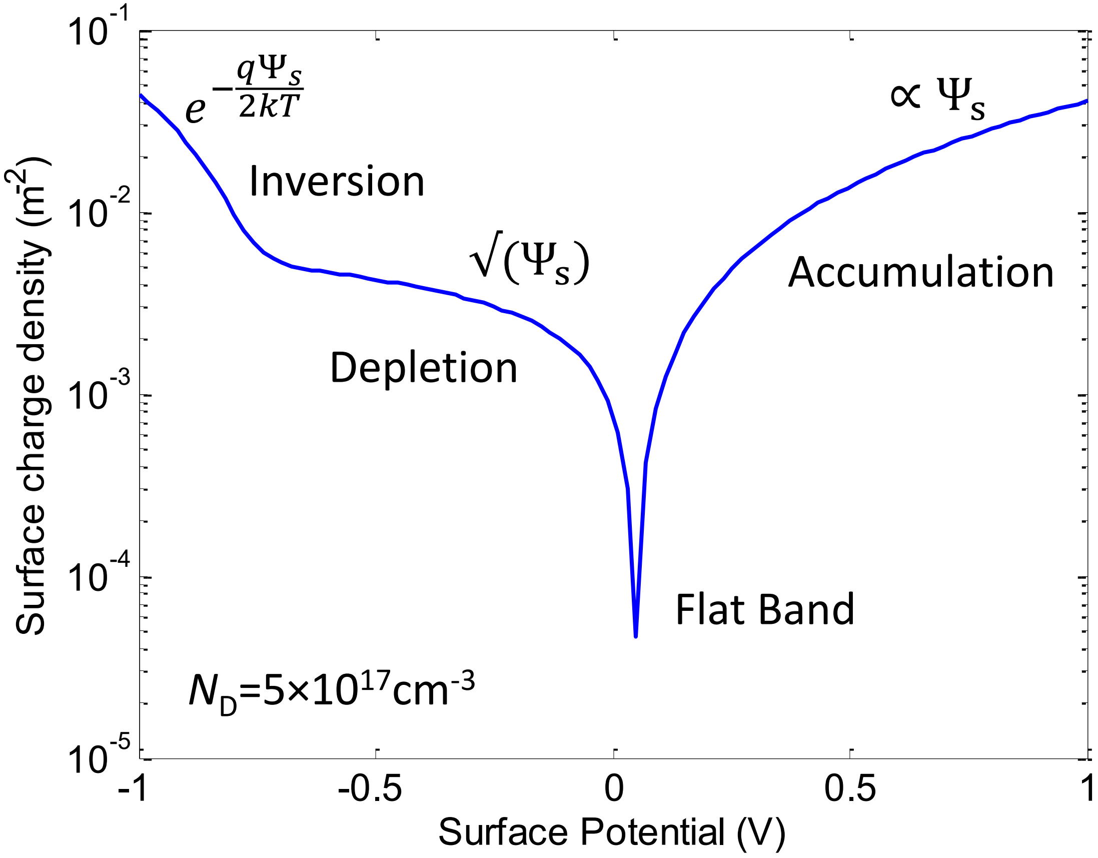
Model below V_T

$$n_s = N_{2D} e^{\frac{V_{GS}-V_T}{kT}}$$

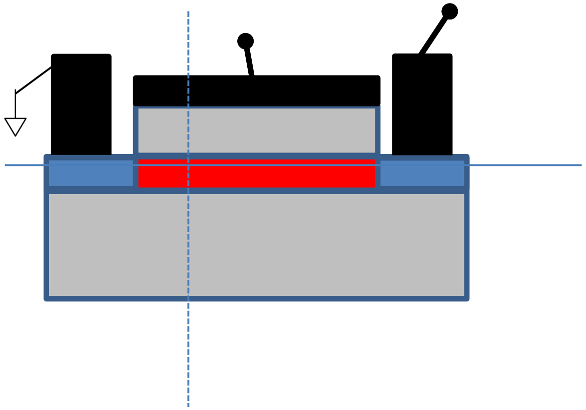
We get two very simple, physically correct and easy to use models accurate below and above V_T.

Typical n-type III-V 3D: Degeneration in accumulation

$$\varepsilon_r(x)\frac{\partial}{\partial x}\varepsilon_r(x)\frac{\partial}{\partial x}\Phi(x) = -\frac{q}{\varepsilon_0}\left(N_d^+ - n(\Phi)\right)$$ Possions Eq.



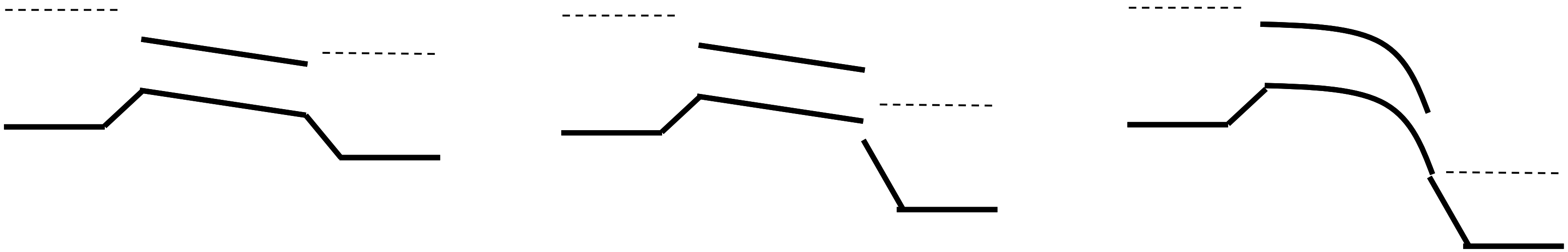
Field Effect Transistors – indirect channel potential control



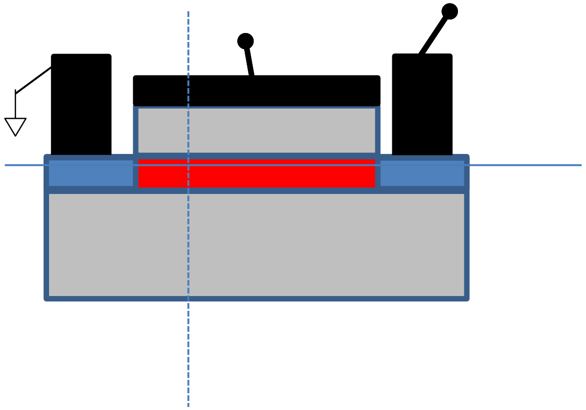
Long channel FET diffusive: potential drop along the channel required.

$$J_{drift} = q\mu_n n(x)\varepsilon(x) = -\mu_n n(x)\frac{dE_c}{dx}$$

Channel potential not 100% controlled by the gate – complicates things. n(x) decreases -> pinch off.



Field Effect Transistors – indirect channel potential control

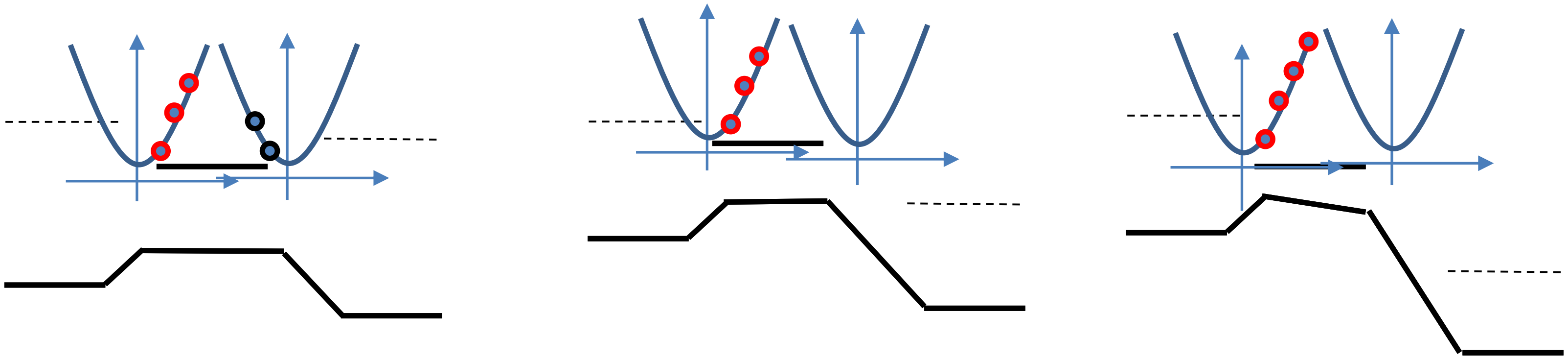


Ballistic FET diffusive: No potential drop along the channel is required

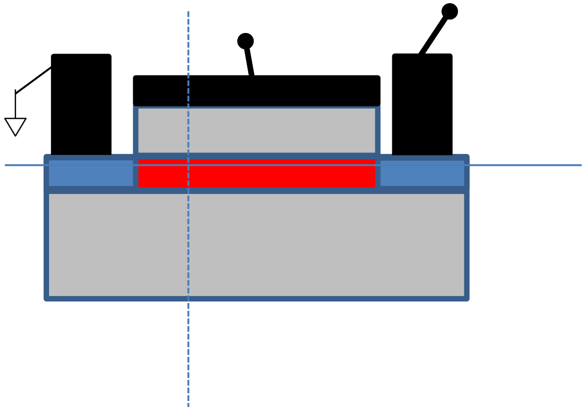
Ideal gate control sets the potential in the channel

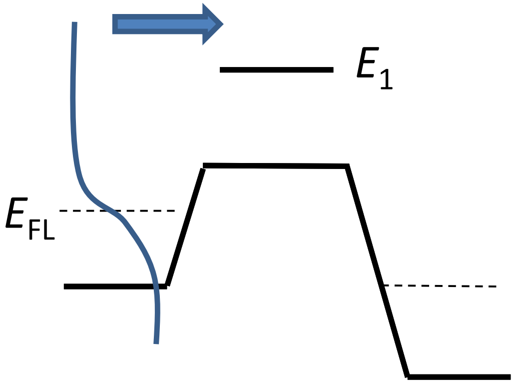
Source/Drain electrodes injects electrons

Short channel effects – large a drain potential can pull down E1 – output conductance



Field Effect Transistors – subthreshold current





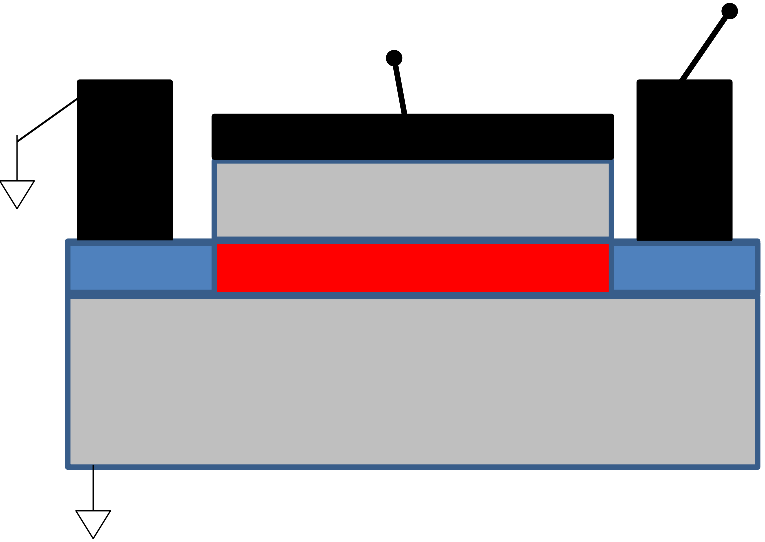
When $E_1 >> E_{F,L}$

- Exponential tail of Fermi-Dirac function:

$$F_j\left(\frac{E_F - E_1}{kT}\right) \approx e^{(E_F - E_1)/kT}$$

- Current decreases exponentially with increasing E_1
- This gives ideally a 60 mV / decade slope
- Theoretical limit for a thermionic switch
- 10^5 on-off ratio: at least 0.3 V_{GS}

Field Effect Transistors – Short Channel Effects

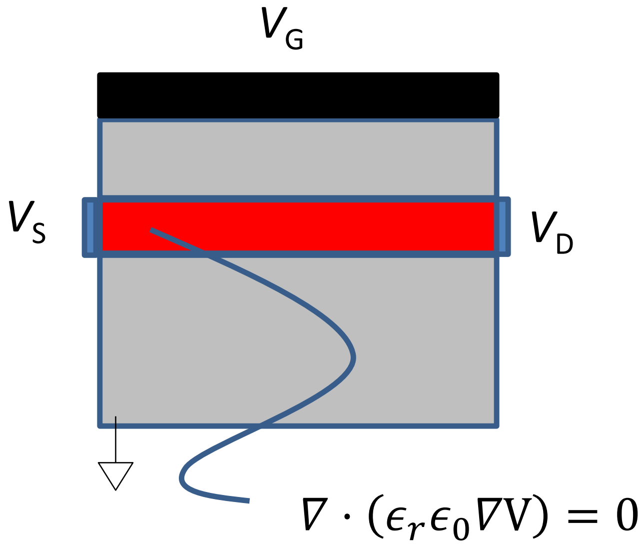


1) We want the channel potential to be set by the gate voltage.

2) When the current through the transistor is small – very little charge inside the channel. $\rho \approx 0\ C/m^2$. (For simplicity here)

$$\nabla \cdot (\epsilon_r \epsilon_0 \nabla \mathrm{V}) = 0$$

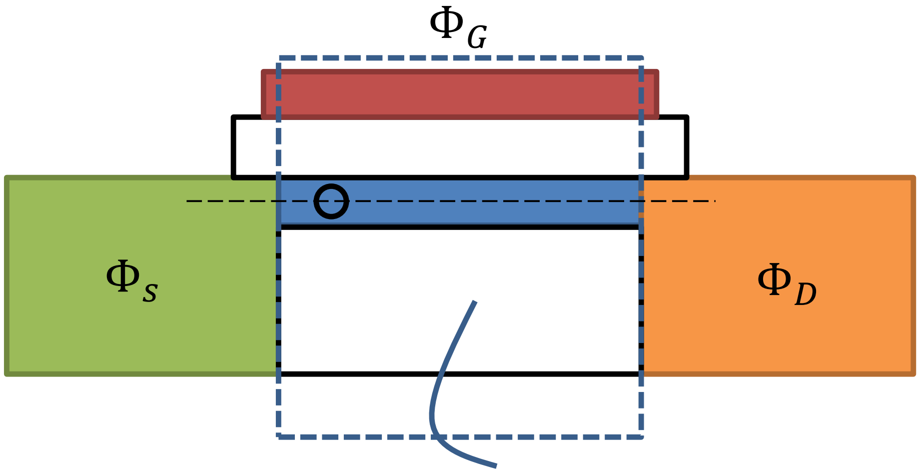
3D Possion equation



3) Both drain, source and gate terminal can influence the potential inside the channel!

4) This is studied by solution to the 2D Possion Equation.

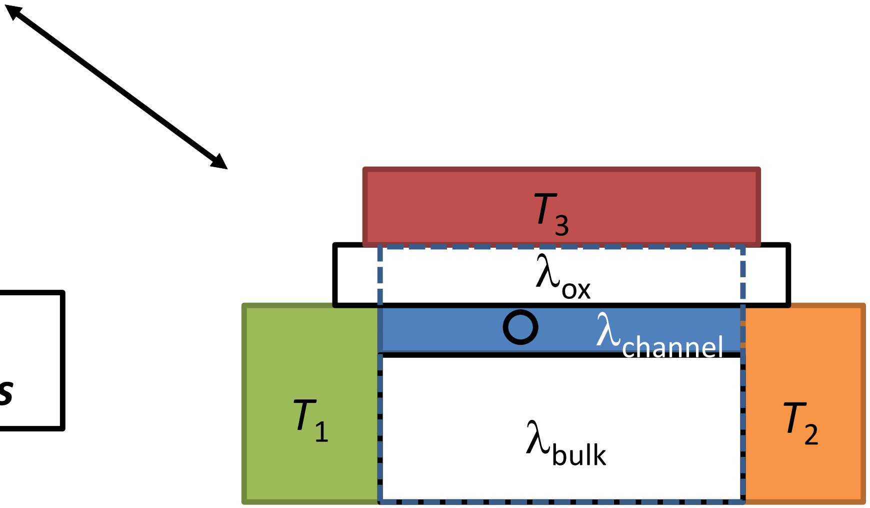
2D Electrostatics – below threshold



$$\nabla\cdot(\epsilon_r\epsilon_0\nabla\Phi)=\rho(\Phi)\approx qN_A$$

Thermal conduction: $\nabla\cdot(\lambda\nabla T)=0$

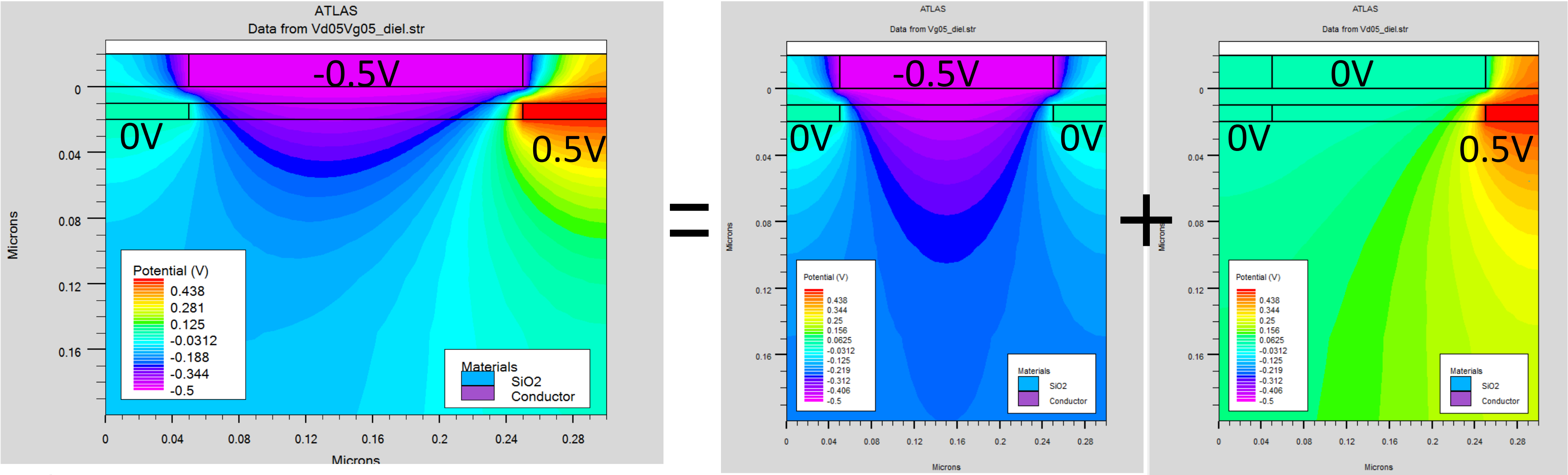
Electrostatics: $\nabla\cdot(\epsilon_r\epsilon_0\nabla\Phi)=0$



$$\nabla\cdot(\lambda\nabla T)=0$$

Laplace's equation for electrostatics:
One to one analogue to thermal gradients

Superposition



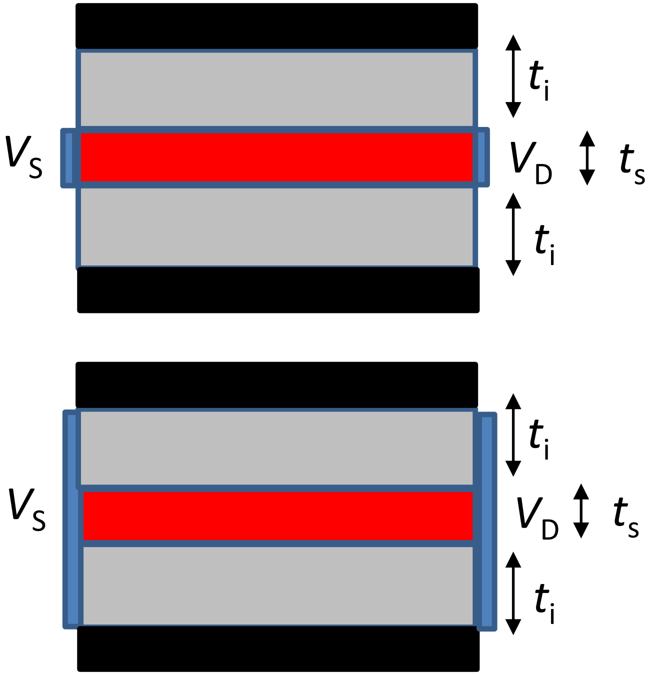
$$\left\{\begin{array}{l}\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}\right)(\alpha\Phi)=\alpha\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}\right)(\Phi)=0\\ \Phi(V_G,V_S,V_D)=\Phi(V_G,0,0)+\Phi(0,V_S,0)+\Phi(0,0,V_D)\end{array}\right.$$

Linear boundary value problem

The potential at a certain point: $\Phi(x,y)=\alpha_G(x,y)V_G+\alpha_D(x,y)V_D+\alpha_S(x,y)V_S$

$0<\alpha_{G,D,S}<1$ x,y dependence from solution of Laplace's equation

Potential Distribution – Double gate FET



$$\nabla \cdot (\epsilon_r \epsilon_0 \nabla V) = 0$$

This can be solved easily with e.g. COMSOL.

Analytical solution through e.g. separation of variables + Fourier series expansion.

$$\frac{t}{\pi} = \lambda$$

$$V(x,y) = \sin\left(\frac{\pi k y}{t}\right) \sum_{k=1}^{\infty} a_k e^{\left(\frac{\pi k x}{t}\right)} + b_k e^{\left(-\frac{\pi k x}{t}\right)}$$

For V_g=0V and $\varepsilon_s \approx \varepsilon_{ox}$.

Keeping only first term

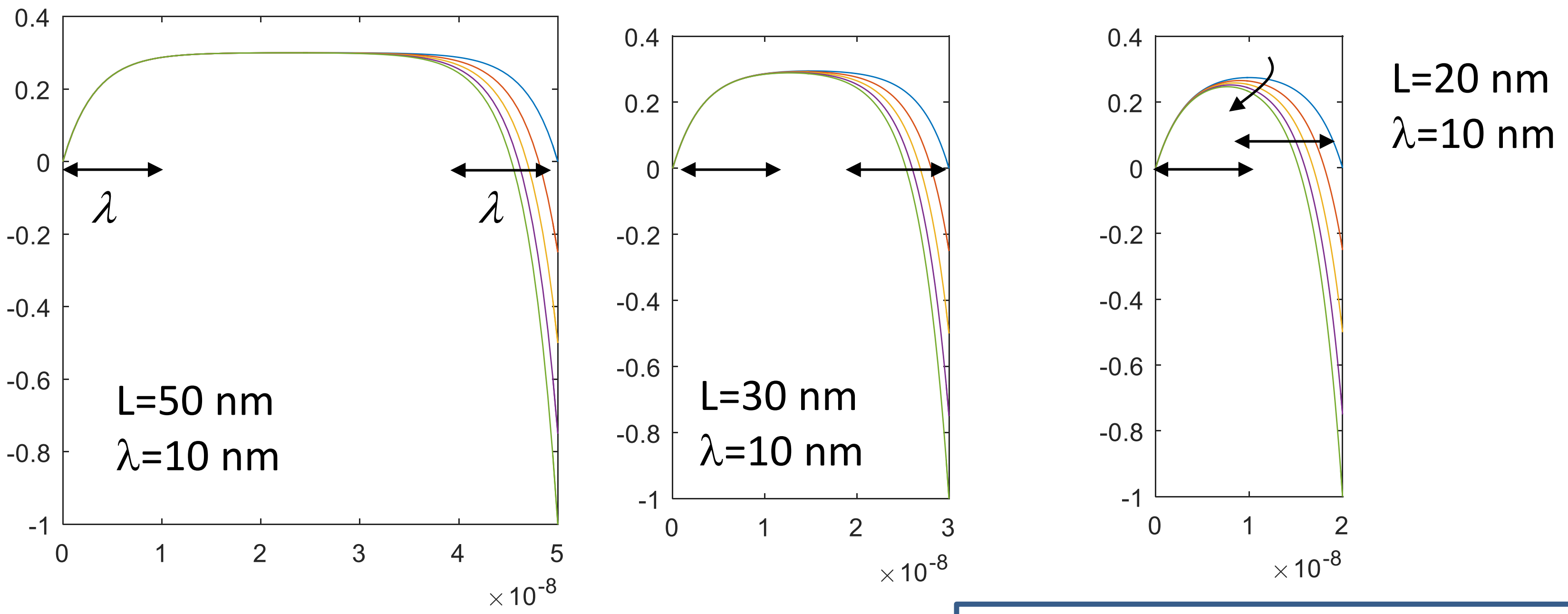
$\lambda \approx (t_s + 2t_i)/\pi$ If $\varepsilon_s \approx \varepsilon_{ox}$ and $t_s >> t_i$

Well behaved FET has: $L_g > 4\lambda$

Geometric Length Scale for the FET

$$V(x) \approx -V_{GS} + V_{GS} \sinh\left(\frac{\pi(L-x)}{\lambda}\right) / \sinh\left(\frac{\pi L}{\lambda}\right) + (V_{DS} + V_{GS}) \sinh\left(\frac{\pi(L-x)}{\lambda}\right) / \sinh\left(\frac{\pi L}{\lambda}\right)$$

Short Channel Effects



$\lambda \approx (t_s + 2t_i)/\pi$ L > 4λ

Short gate lengths requires **thin oxide** and **thin semiconductors**

Double Gate

$$\lambda_{GAA} < \lambda_{DG} < \lambda_{SG}$$

Gate All Around Single Gate

FinFETs/Nanowire: thicker t_i/t_s for the same gate length

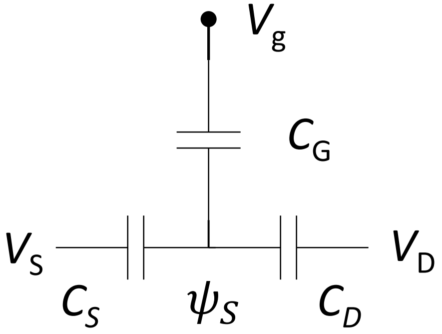
2D Electrostatics – Capacitance model

Stored charge

$$\psi_s = \left(\frac{C_G}{C_\Sigma}V_G + \frac{C_D}{C_\Sigma}V_D + \frac{C_S}{C_\Sigma}V_S\right) + \frac{Q(\psi_s)}{C_\Sigma}$$

$$C_\Sigma = C_S + C_D + C_G$$

$$\delta Q_s = -C_q(\psi_s)\delta\psi_s$$



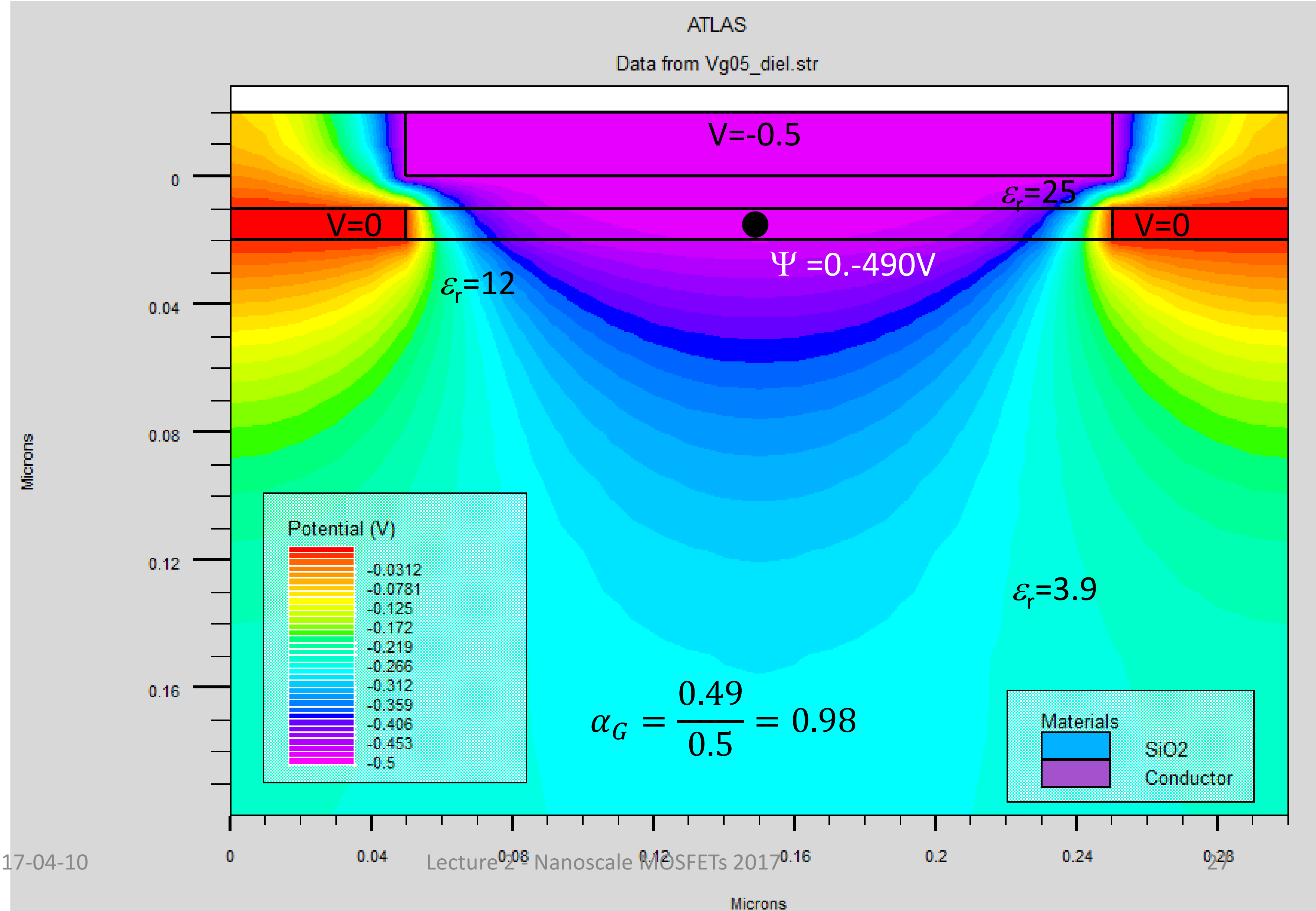
Top of the barrier - potential

$$\alpha_D = \frac{C_D}{C_\Sigma}$$ DIBL & output conductance

$$\alpha_G = \frac{C_G}{C_\Sigma}$$ Subthreshold slope & transconductance

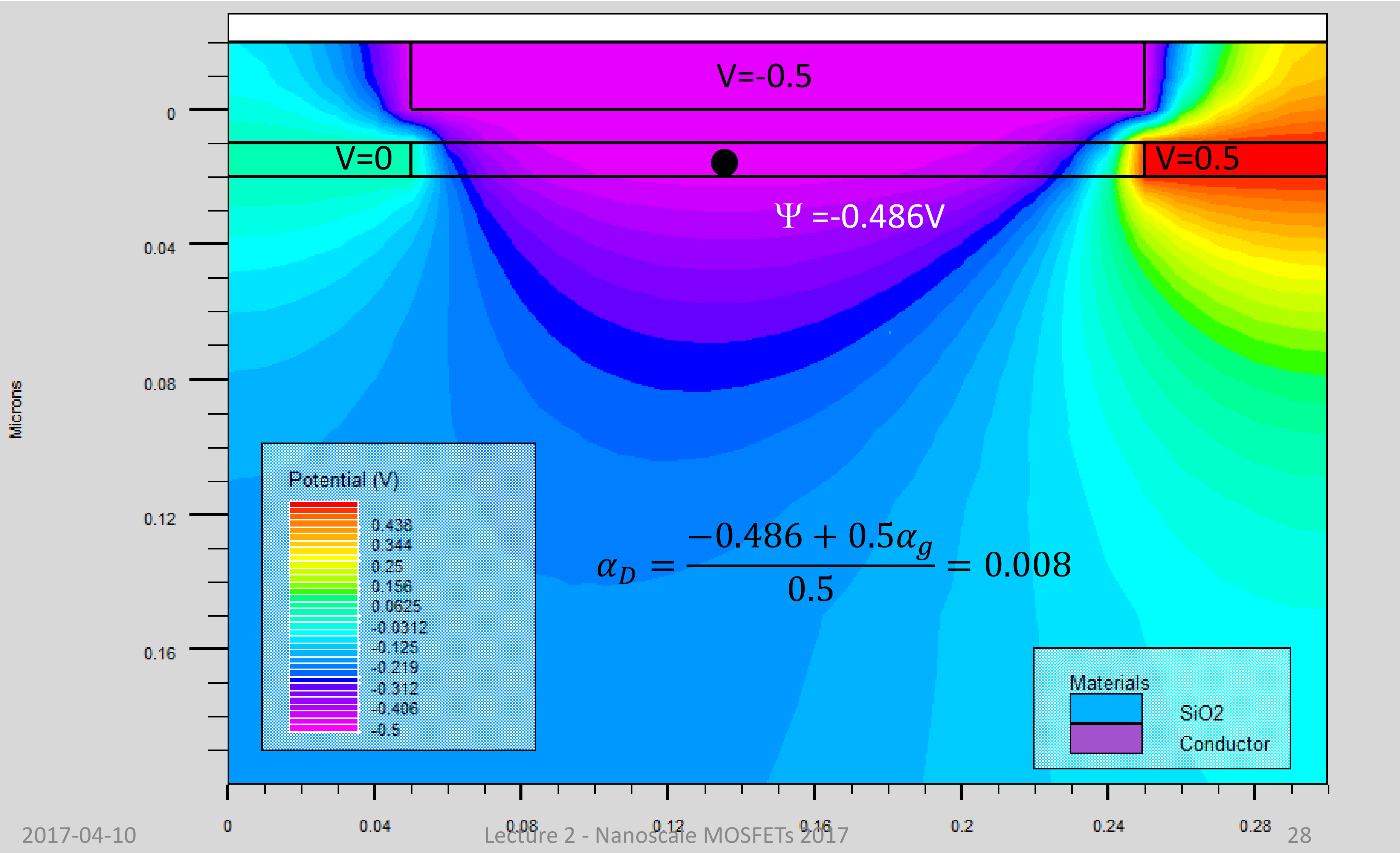
You will derive this as an excercises

2D FET Potential Example: SOI V_{GS}= -0.5 V



$$\alpha_G = \frac{0.49}{0.5} = 0.98$$

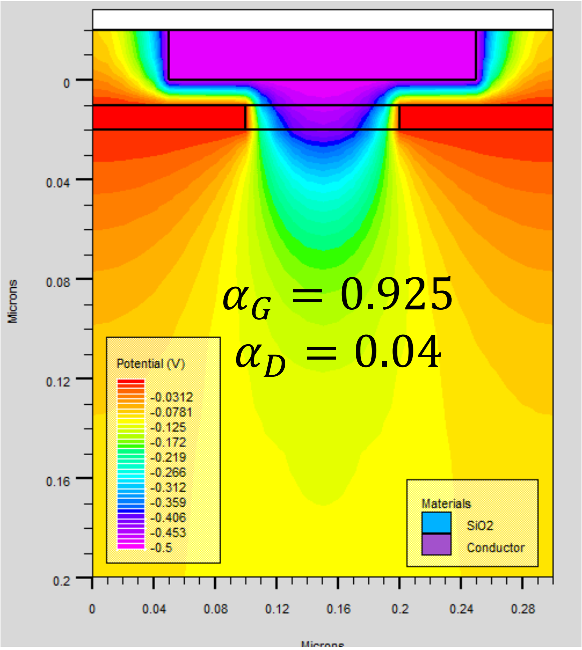
2D FET Potential: V_{GS}= -0.5 V; V_{DS}=0.5V



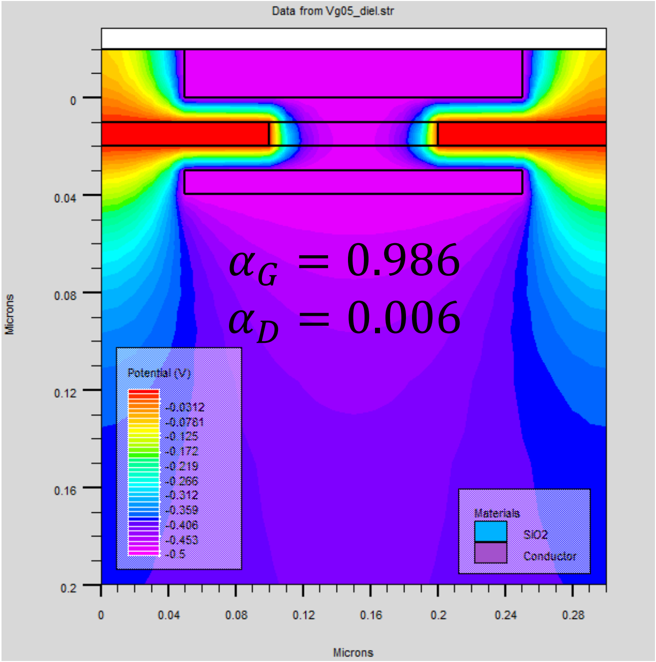
$$\alpha_D = \frac{-0.486 + 0.5\alpha_g}{0.5} = 0.008$$

2D FET Potential: $L_G = 100$ nm

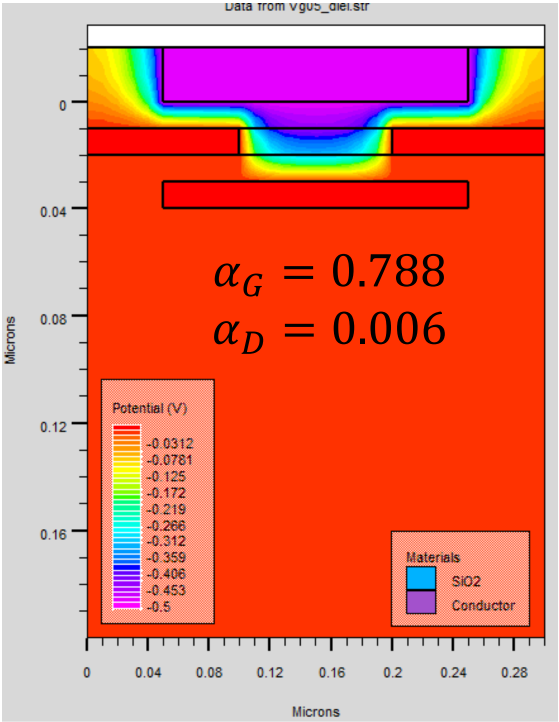
Single Gate



Double Gate



Ground Plane



Thinner C_{ox}, higher ε_r
Multiple gates
Thinner channel, lower ε_r

Higher α_G, Lower α_D

Back barrier ground plane

Lower α_G **Lower α_D**

$$\nabla \cdot (\lambda \nabla T) = 0$$

$$\nabla \cdot (\epsilon_r \epsilon_0 \nabla \Phi) = 0$$

Diffusive MOSFETs – current models

$$\boxed{I_D = -WQ(0)\langle v(0)\rangle}$$

General equation for a barrier controlled device

$$I_D = -WQ(0)\langle v(0)\rangle = WC_{GS}(V_{GS} - V_T)\langle v(0)\rangle \qquad \alpha_G \gg \alpha_{D,S}$$

$$I_D = \frac{W}{L}\mu_{eff}C_{ox}(V_{GS} - V_T)V_{DS}$$

Low field, long (diffusive) channel

$$I_{Dsat} = \frac{W}{2L}\mu_{eff}C_{ox}(V_{GS} - V_T)^2$$

High field, long channel

$$I_{Dsat} = Wv_{sat}C_{ox}(\mathrm{V_{GS}} - \mathrm{V_T})$$

High field, velocity saturation (short channel)

$$I_{D,subth} = \frac{W}{L}(m-1)\mu_{eff}C_{ox}\left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{GS}-V_T)}{mkT}} \propto e^{\frac{q}{kT}\left[\frac{C_G}{C_\Sigma}V_G + \frac{C_D}{C_\Sigma}V_D\right]}$$

Sub threshold – ’weak inversion’