Lecture 5 – Scattering & Interface Defects

- Scattering
- Transmission
- Interface defects

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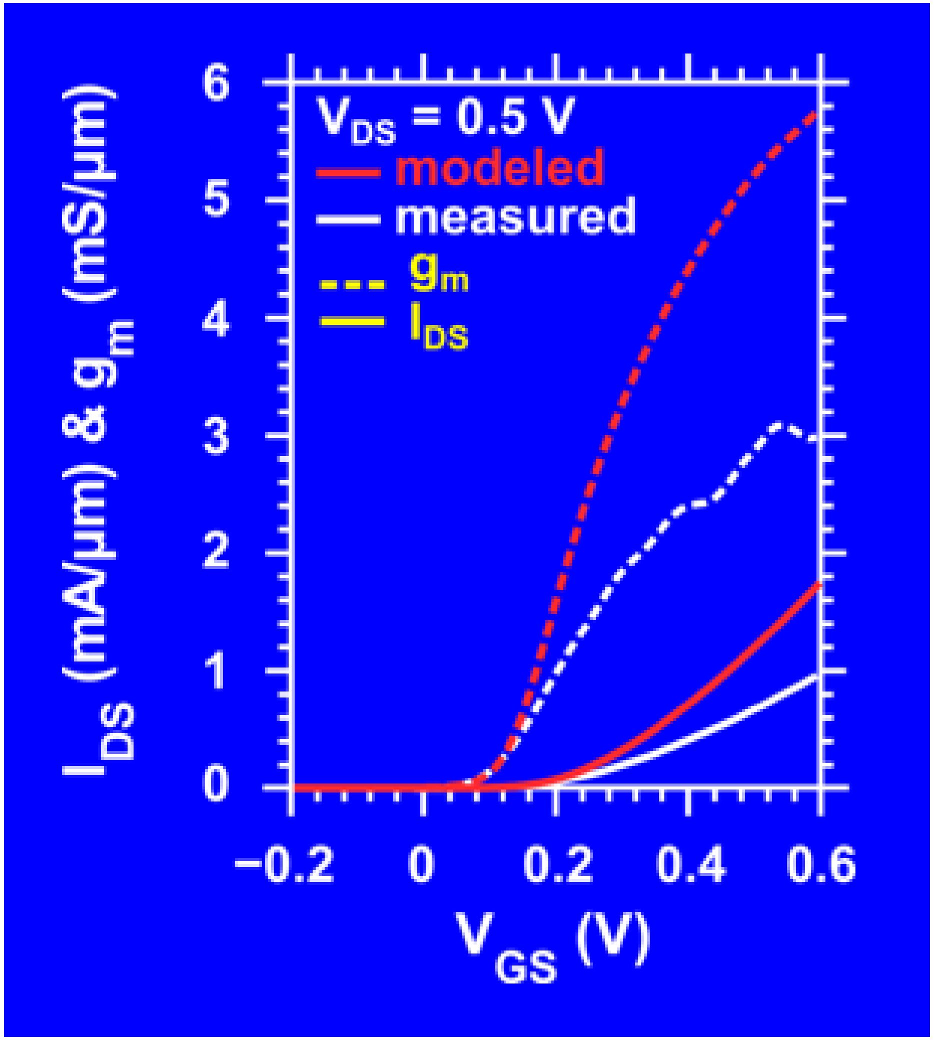
Best Transistors:
g_m 3-3-3.45 mS/µm @ v_{DS}=0.5V

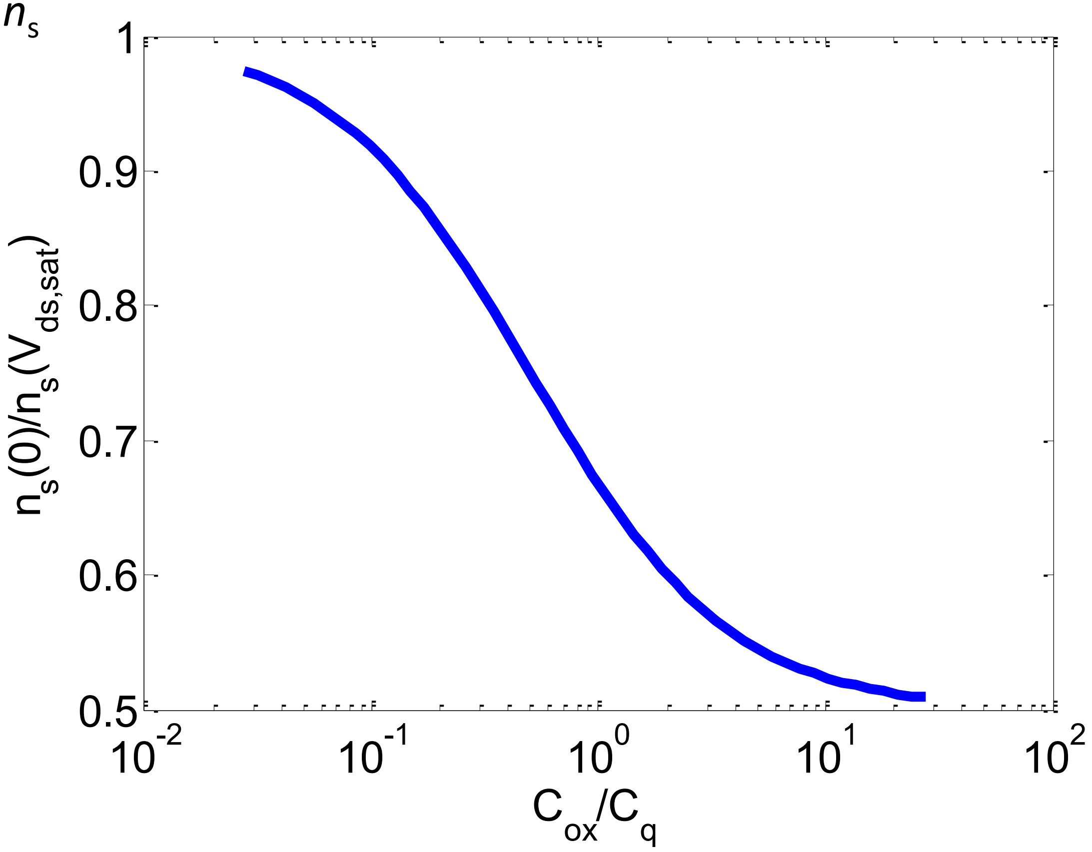
Fully Ballistic model: ~ 6 mS/µm



C.B. Zota, IEDM 2016

MOS/Bipolar(QCL) Limits

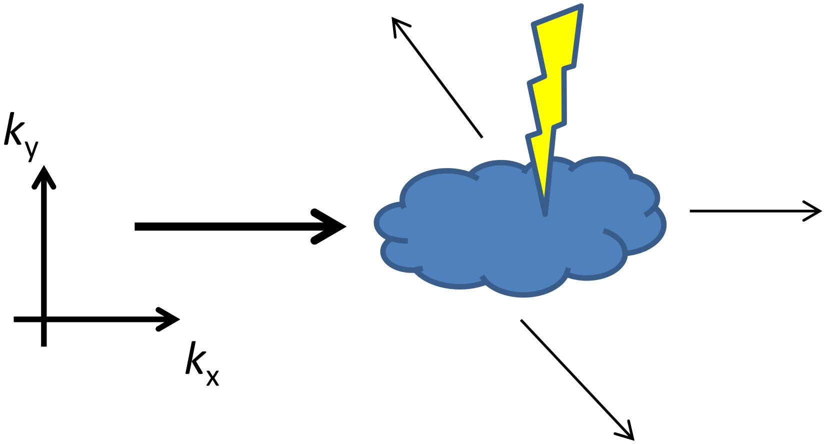
MOS Limit: $C_{ox} \ll C_q$: V_G controlls n_s directly



QCL Limit: $C_{ox} \gg C_q$: V_G controlls $\varepsilon(0)$ directly

Scattering

- Ionized Impurities
- Phonons
- Surface Roughness
- Electron/electron



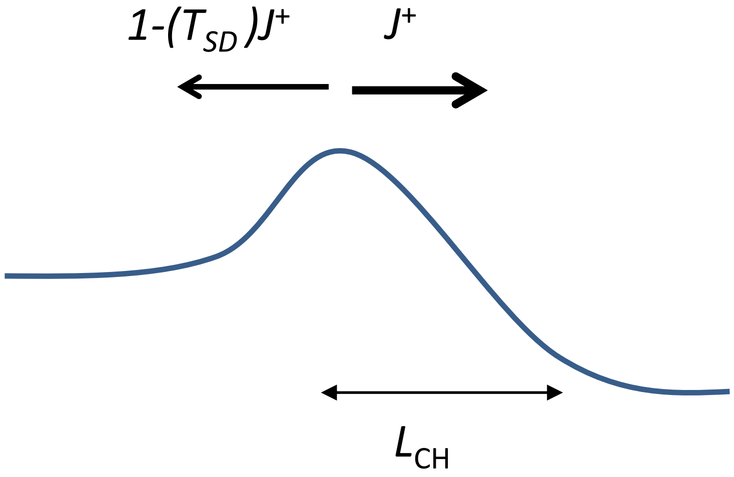
Basic scattering theory (Fermi's golden rule) – scattering rates are proportional to DOS

$$\boxed{\begin{array}{l} \dfrac{1}{\tau} \propto D_{nD}(E) \\[2em] \lambda_0 = v_T \tau \end{array}}$$

Elastic Scattering (Impurities): Conserve energy of the electron / randomizes momentum

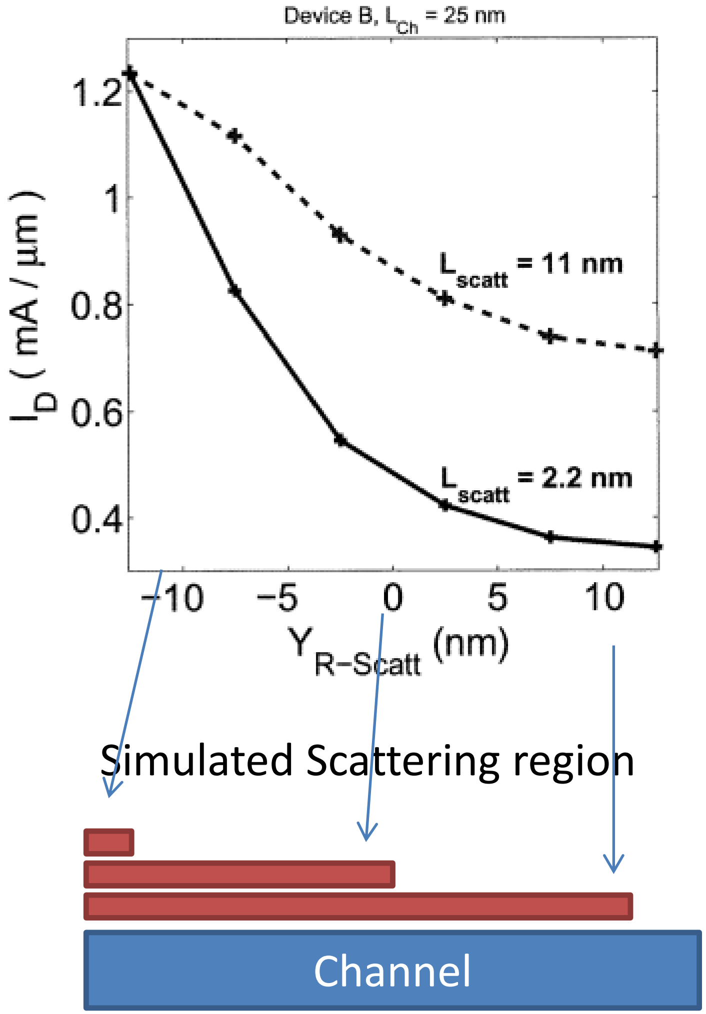
Inelastic Scattering (Phonons): Energy and momentum is not conserved – absorbtion/emmission of phonons.

Effect of scattering:



$0 \leq T_{SD} \leq 1$

- Mixes n+ and n- states
- Most important close to the source edge
- Lowers current

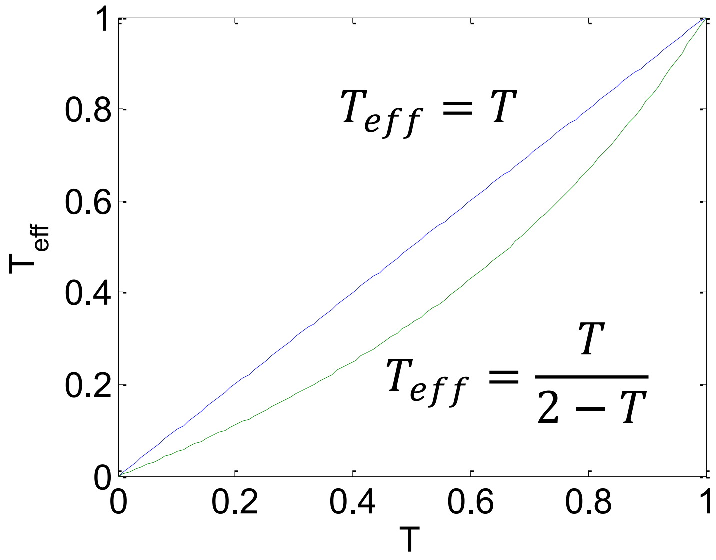


Current with scattering

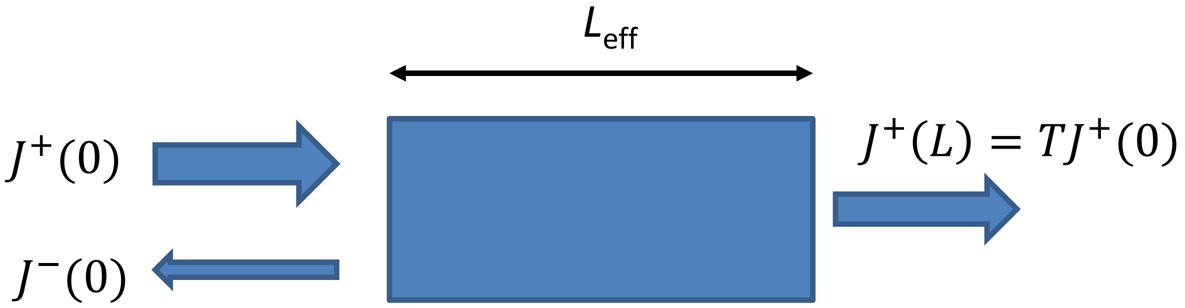
$I_D = T(I^+ - I^-)$ Linear Regieme

$$I_{D,scattering} = \frac{T}{2-T}(I^+ - I^-)$$ MOS Limit

$$I_{D,scattering} = T(I^+ - I^-)$$ QCL Limit



Transmission under low drain bias



J: flux of carriers

$$T = \frac{\lambda_0}{\lambda_0 + L}$$

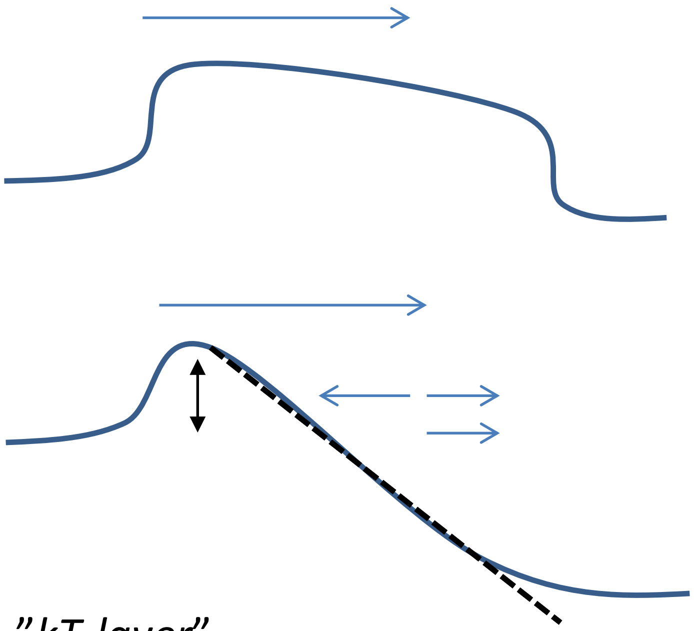
Low field limit

$$D_n \equiv \frac{\lambda_0 v_T}{2} = \frac{kT_L}{q}\mu_{eff}$$

Low field, non degenerate

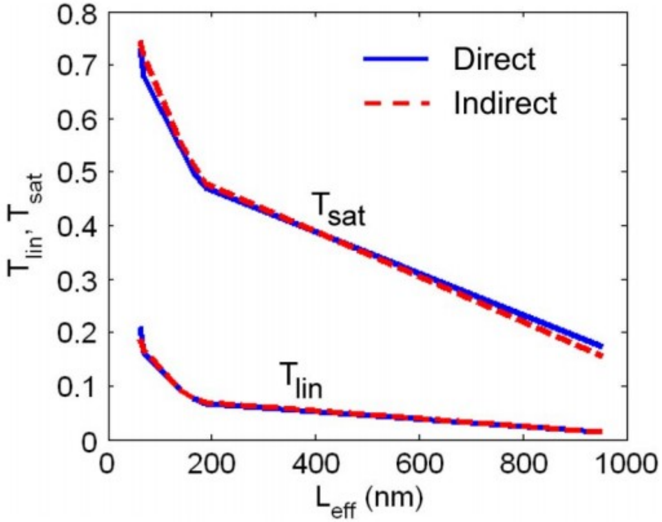
Low/High Bias

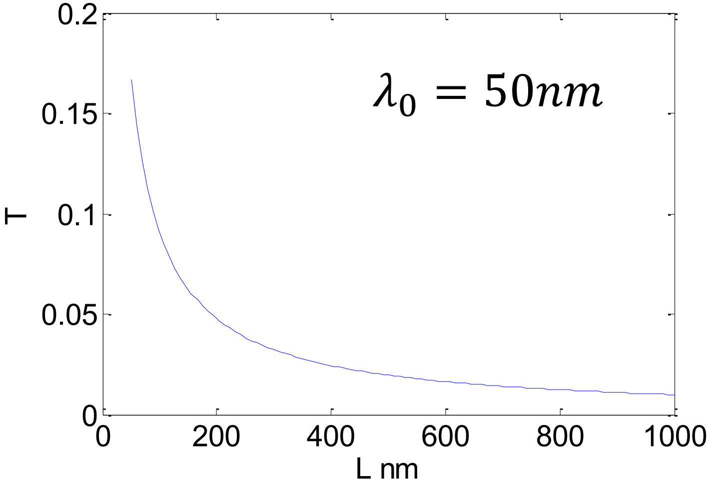
Large V_{DS} shows much higher T – smaller probability of back scattering.



"kT-layer"

$$l \approx \frac{kT}{qV_{DS}} L \ll L \quad \longrightarrow \quad T = \frac{\lambda_0}{\lambda_0 + l}$$





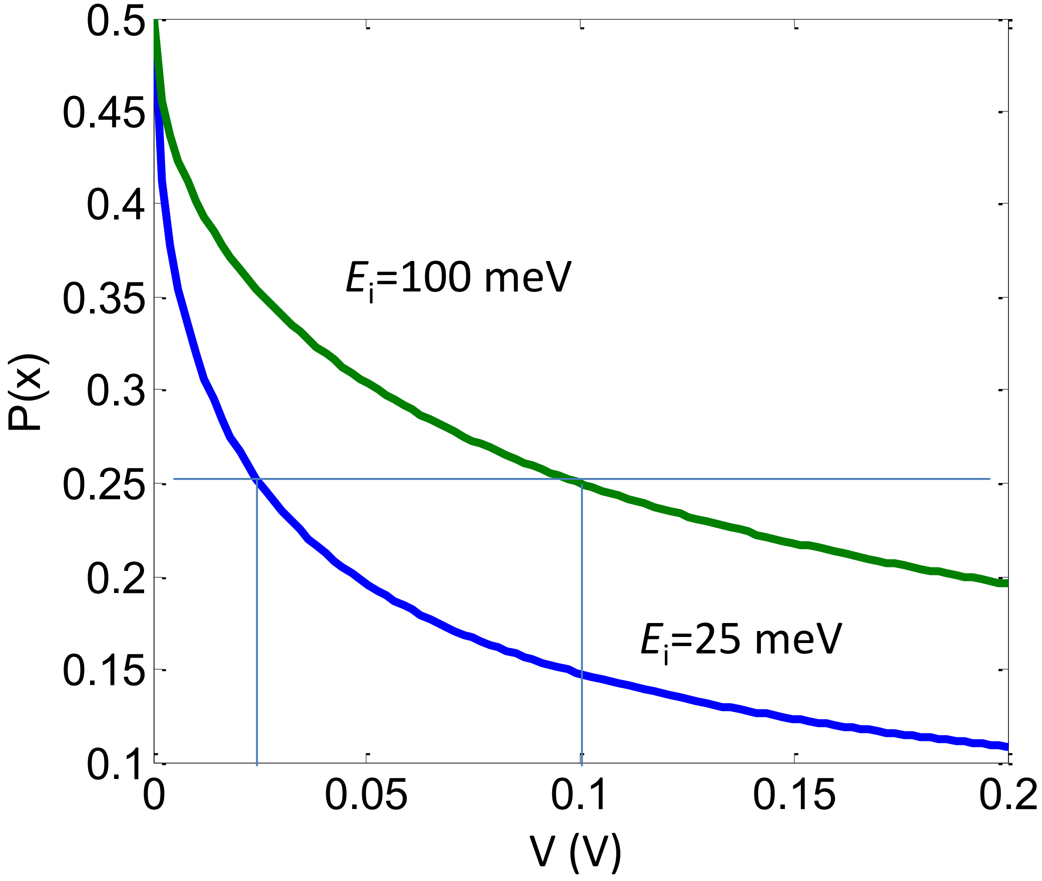
Backscattering probability

$$P(x) = \frac{1}{\pi}\cos^{-1}\sqrt{\frac{qV(x)}{qV(x) + (E_i - E_b)}}$$

Non-degenerate carriers have E_i ~kT

”Small” probability of back scattering for V>0.025V : *kT-layer*

Degenerate carriers have higher E_i – this leads to longer effective lengths for scattering



Interface traps

Acceptor Traps: 0/- (Empty/Charged)

Donor Traps: +/0 (Empty/Charged)

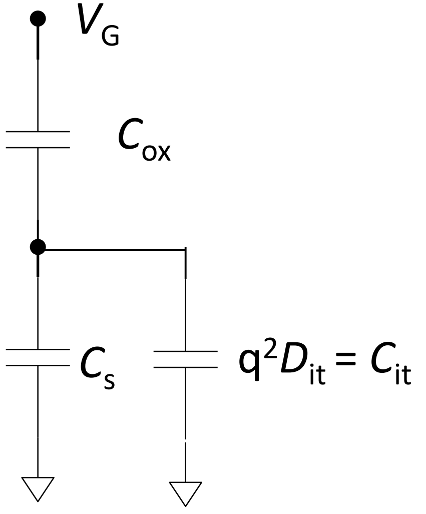
$$\frac{Q_{it}}{q} = \int_{-\infty}^{+\infty} D_{it}^{don}(E) f_d(E_F) dE + \int_{-\infty}^{+\infty} D_{it}^{acc}(E)(1 - f_d(E_F) dE$$

$$C_{it} = \frac{\partial Q_{it}}{\partial \psi_s} = -q^2 \frac{\partial Q_{it}}{\partial \varepsilon(0)}$$

$$C_{it} \approx q^2 \, D_{it}(\psi_s)$$

T=0K approximation or
D_{it} constant around E_F

Interface/oxide traps



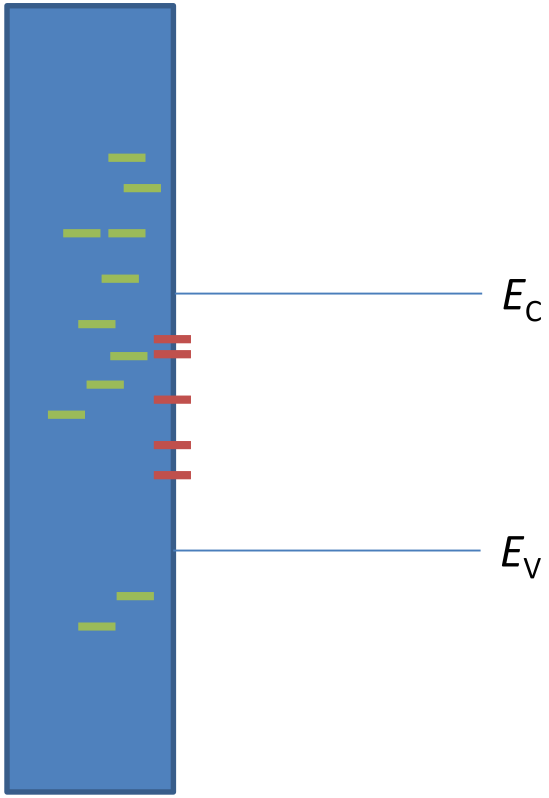
$$\delta\varepsilon(0) = \frac{C_{ox}}{C_s + C_{it}} \delta V_G$$

D_{it} : (eV^{-1} cm^{-2})

10^{10}
10^{11}-10^{14} (III-V)

A very large D_{it} is sometimes called ”Fermi Level Pinning”

Interface / Border Traps



Traps at the SI – interface : Interface Traps

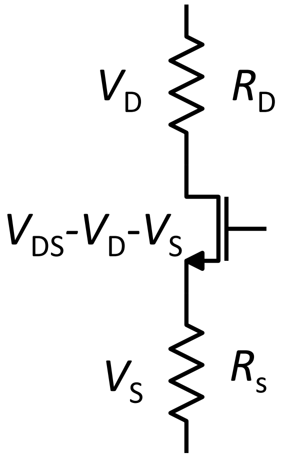
- Only (really) well defined inside the band gap. Can be well modeled using SRH.
- (Conductance method)

Traps inside the oxide – Border Traps

- N_{BT}: (cm^{-3} eV^{-1}).
- SRH + WBK

- More complicate electrostatics
- ’Project’ traps to the interface.
- (Aein’s Thesis)

Other degradation sources



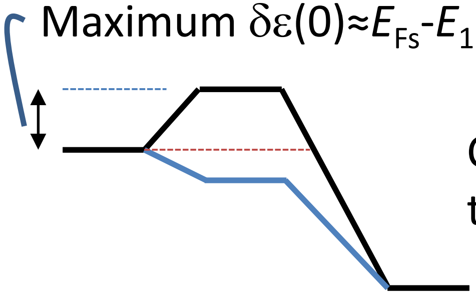
Source/Drain Resistance

$$g_m = \frac{g_{mi}}{1 + g_{mi}R_S + g_{di}(R_S + R_D)}$$

$$g_d = \frac{g_{di}}{1 + g_{mi}R_S + g_{di}(R_S + R_D)}$$

Larger V_{DS} needed to get transistor into saturation

Source Starvation


Maximum $\delta\varepsilon(0) \approx E_{Fs}-E_1$

Can not supply more carriers then there are in the source!